

## BY-MG12864DLYS-06P

### Product

**Standard LCD module**  
**128 x 64 dots graphic type**  
**Normal temperature**  
**STN yellow/green LCD**  
**COG bonding type**  
**With yellow/green color led side light**

Version	Prepared / Date	Approved / Date
0.0	ZhangHong 22/7-2004	David Yu 22/7-2004
A	ZhangHong 11/8-2004	David Yu 11/8-2004

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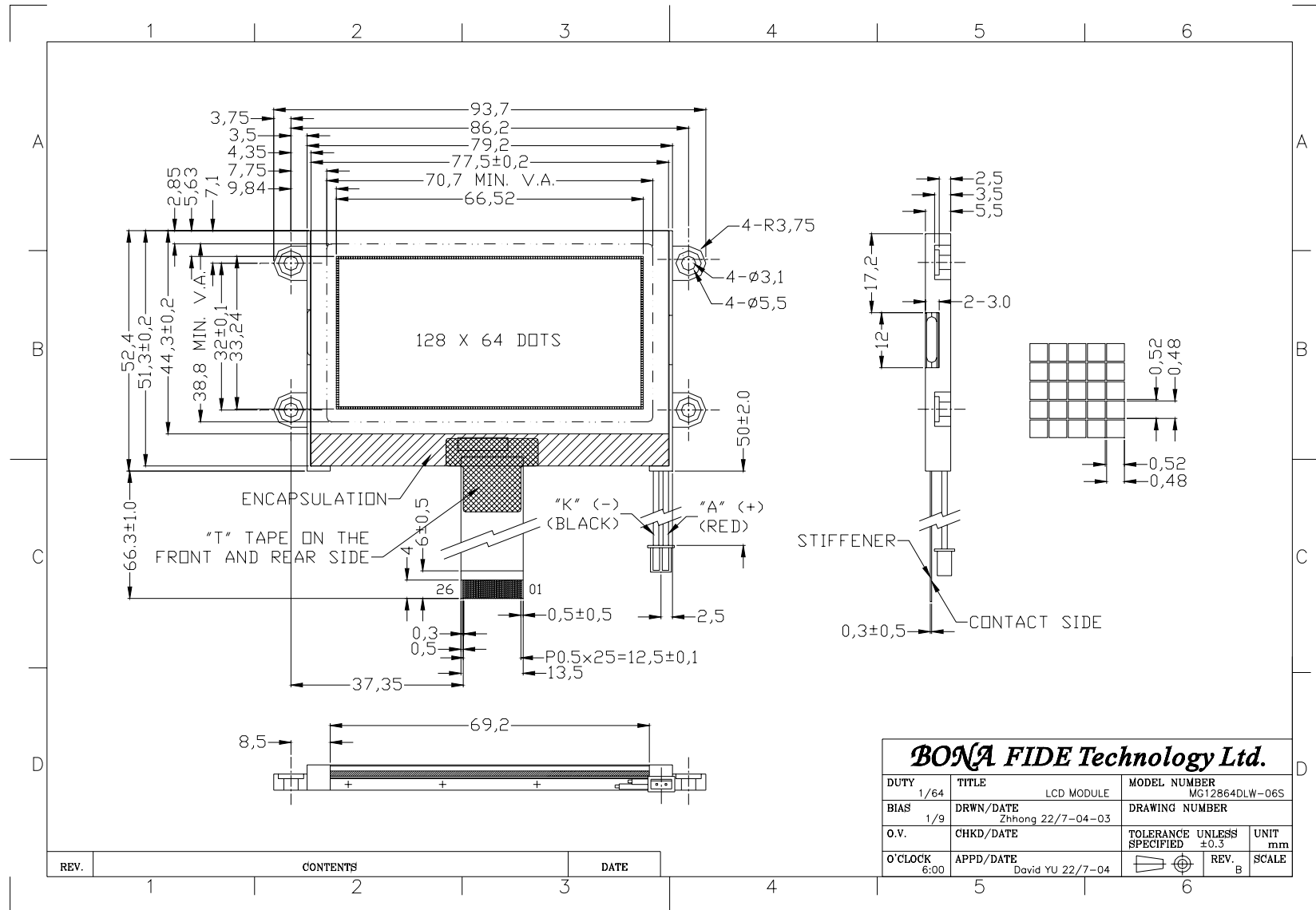
## 1. RECORD OF REVISION

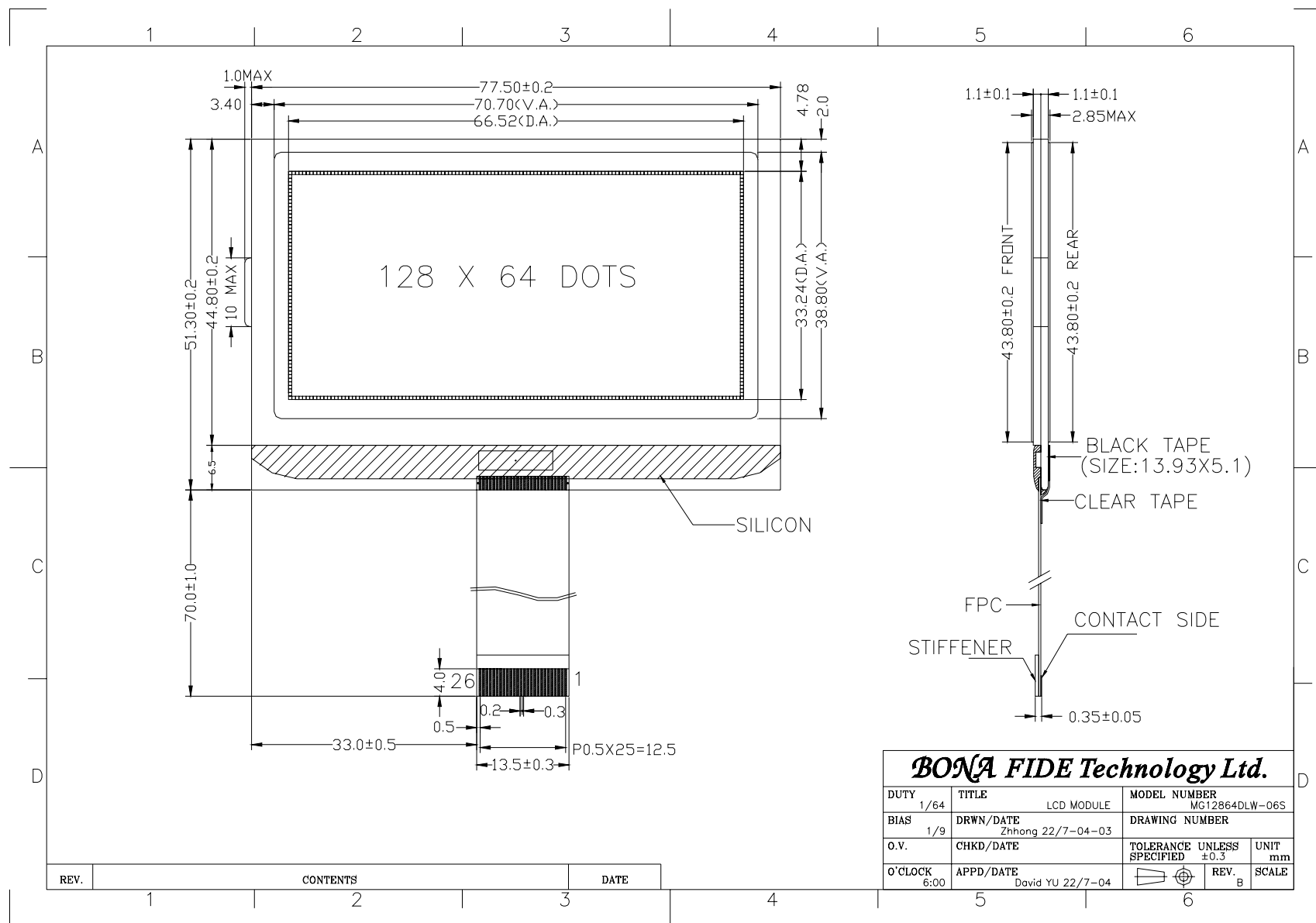
<b>Version</b>	<b>Content</b>	<b>Date</b>
0.0	Original	22/7-04
A	<ol style="list-style-type: none"><li>1. Add structure drawing</li><li>2. Add circuit drawing</li><li>3. Add part list</li></ol>	11/8-04

## 2. PHYSICAL DATA

Item	Contents	Unit
LCD type	STN Y/G	---
LCD duty	1/64	---
LCD bias	1/9	---
Viewing direction	6	O'clock
Module size (W×H×T)	93.7 × 52.4 × 5.5MAX	mm
Viewing area (W×H)	70.7× 38.8	mm
Number of dots	128 × 64	dots
Dot size (W×H)	0.48 × 0.48	mm
Dot pitch (W×H)	0.52 × 0.52	mm
Operation temperature	0 °C ~ 50 °C	---
Storage temperature	-10 °C ~ 60 °C	---

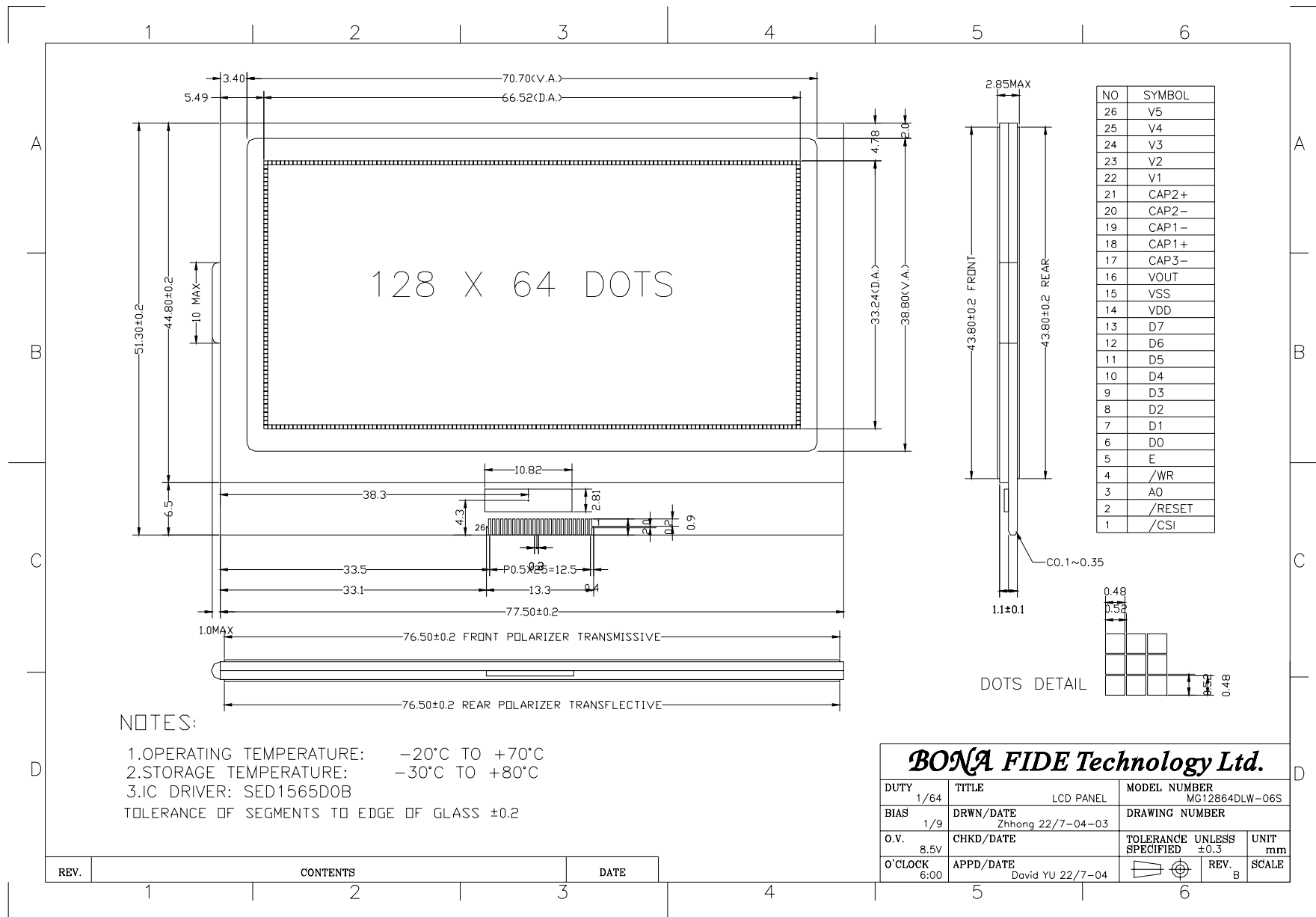
### 3. OUTLINE DIMENSIONS





REV.	CONTENTS	DATE
1		
2		
3		

<b>BONA FIDE Technology Ltd.</b>			
DUTY	TITLE	MODEL NUMBER	
1/64	LCD MODULE	MG12864DLW-06S	
BIAS	DRWN/DATE	DRAWING NUMBER	
1/9	Zhong 22/7-04-03		
O.V.	CHKD/DATE	TOLERANCE UNLESS SPECIFIED	UNIT
		±0.3	mm
O'CLOCK	APPD/DATE	REV.	SCALE
6:00	David YU 22/7-04	B	



NO	SYMBOL
26	V5
25	V4
24	V3
23	V2
22	V1
21	CAP2+
20	CAP2-
19	CAP1-
18	CAP1+
17	CAP3-
16	VOUT
15	VSS
14	VDD
13	D7
12	D6
11	D5
10	D4
9	D3
8	D2
7	D1
6	D0
5	E
4	/WR
3	A0
2	/RESET
1	/CSI

**NOTES:**

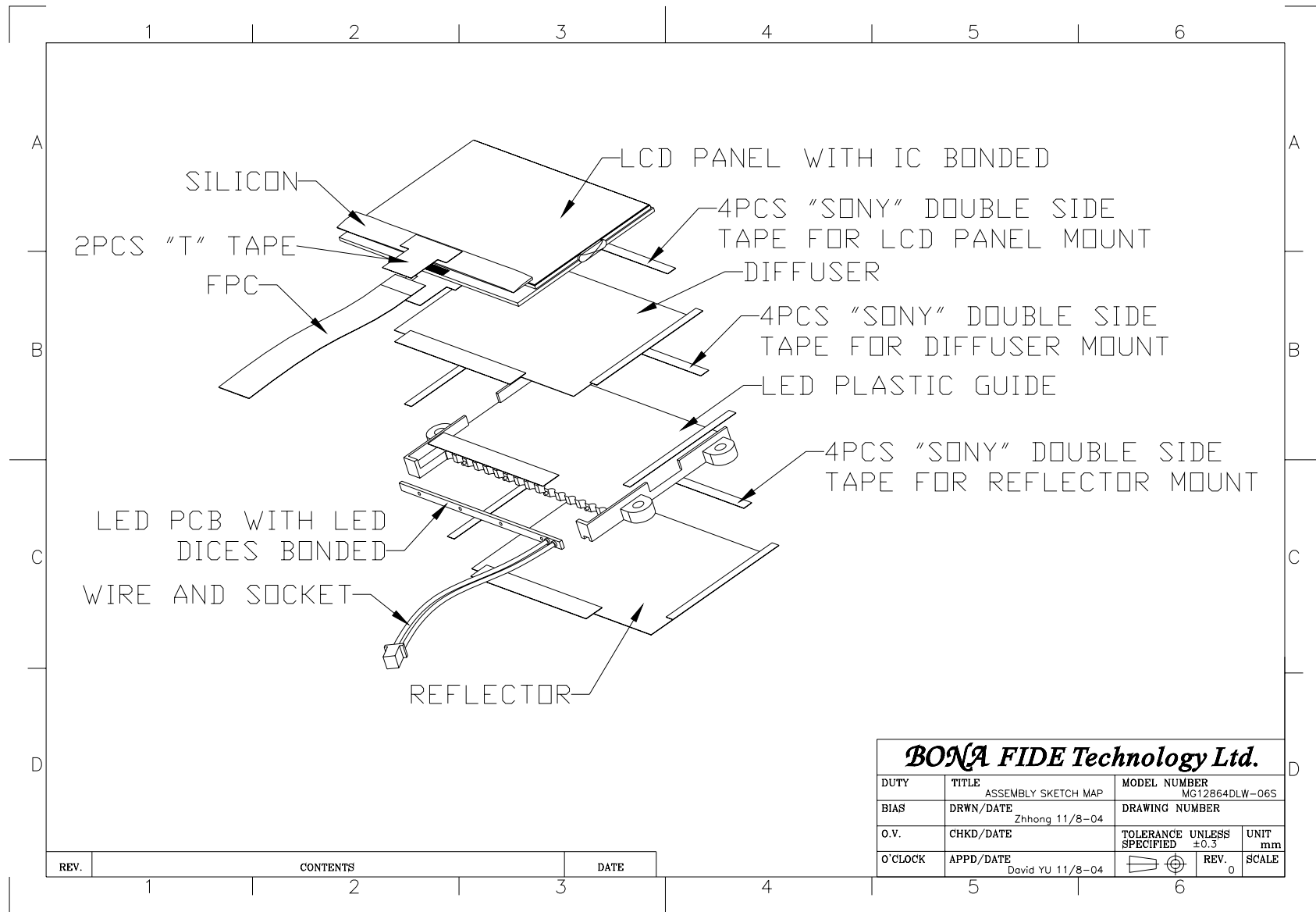
- 1. OPERATING TEMPERATURE: -20°C TO +70°C
  - 2. STORAGE TEMPERATURE: -30°C TO +80°C
  - 3. IC DRIVER: SED1565D0B
- TOLERANCE OF SEGMENTS TO EDGE OF GLASS ±0.2

**BONA FIDE Technology Ltd.**

DUTY	1/64	TITLE	LCD PANEL	MODEL NUMBER	MG12864DLW-06S
BIAS	1/9	DRWN/DATE	Zhhong 22/7-04-03	DRAWING NUMBER	
O.V.	8.5V	CHKD/DATE		TOLERANCE UNLESS SPECIFIED	±0.3
O'CLOCK	6:00	APPD/DATE	David YU 22/7-04	REV.	B

REV.	CONTENTS	DATE
1		
2		
3		

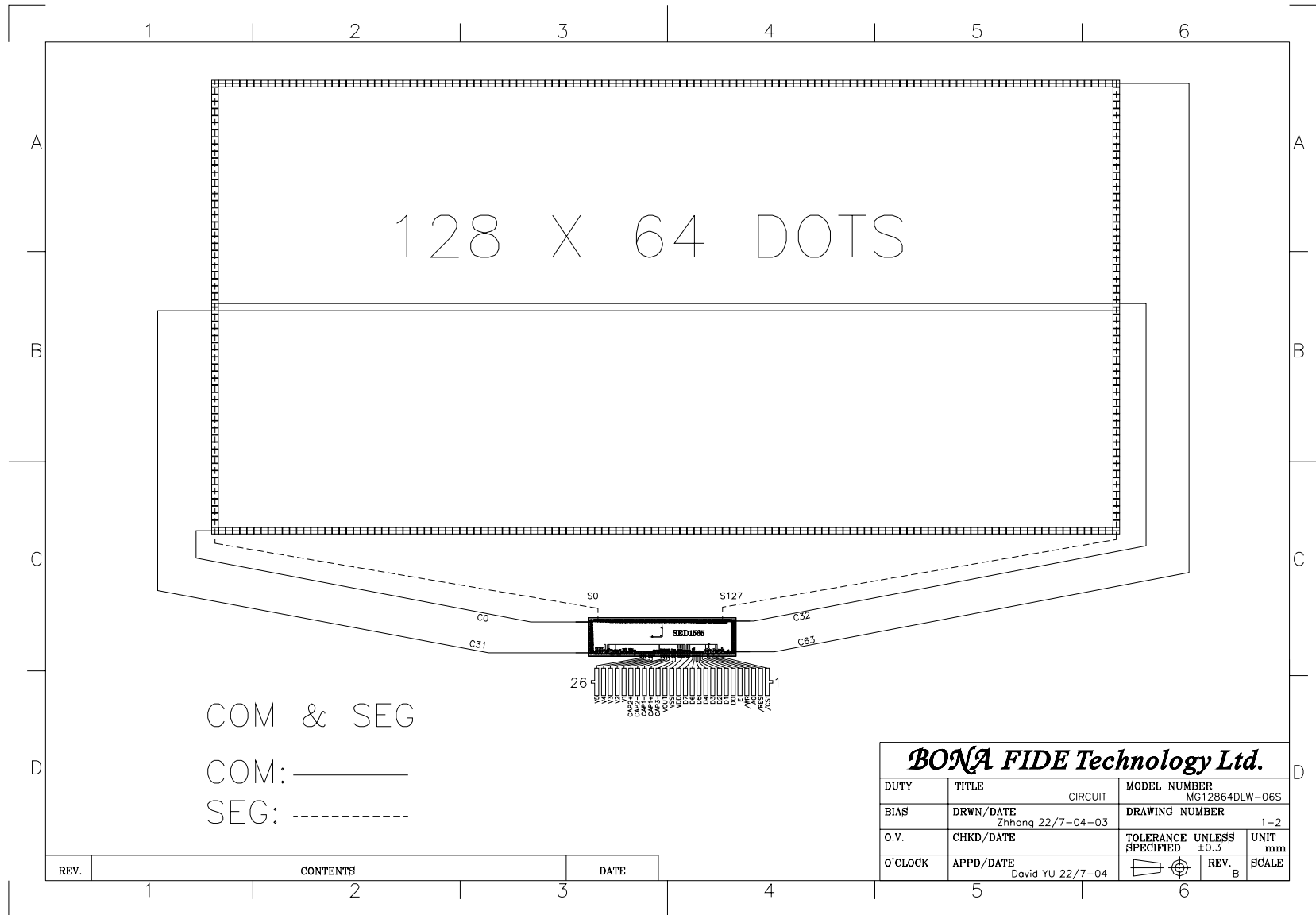
#### 4. ASSEMBLY SKETCH MAP

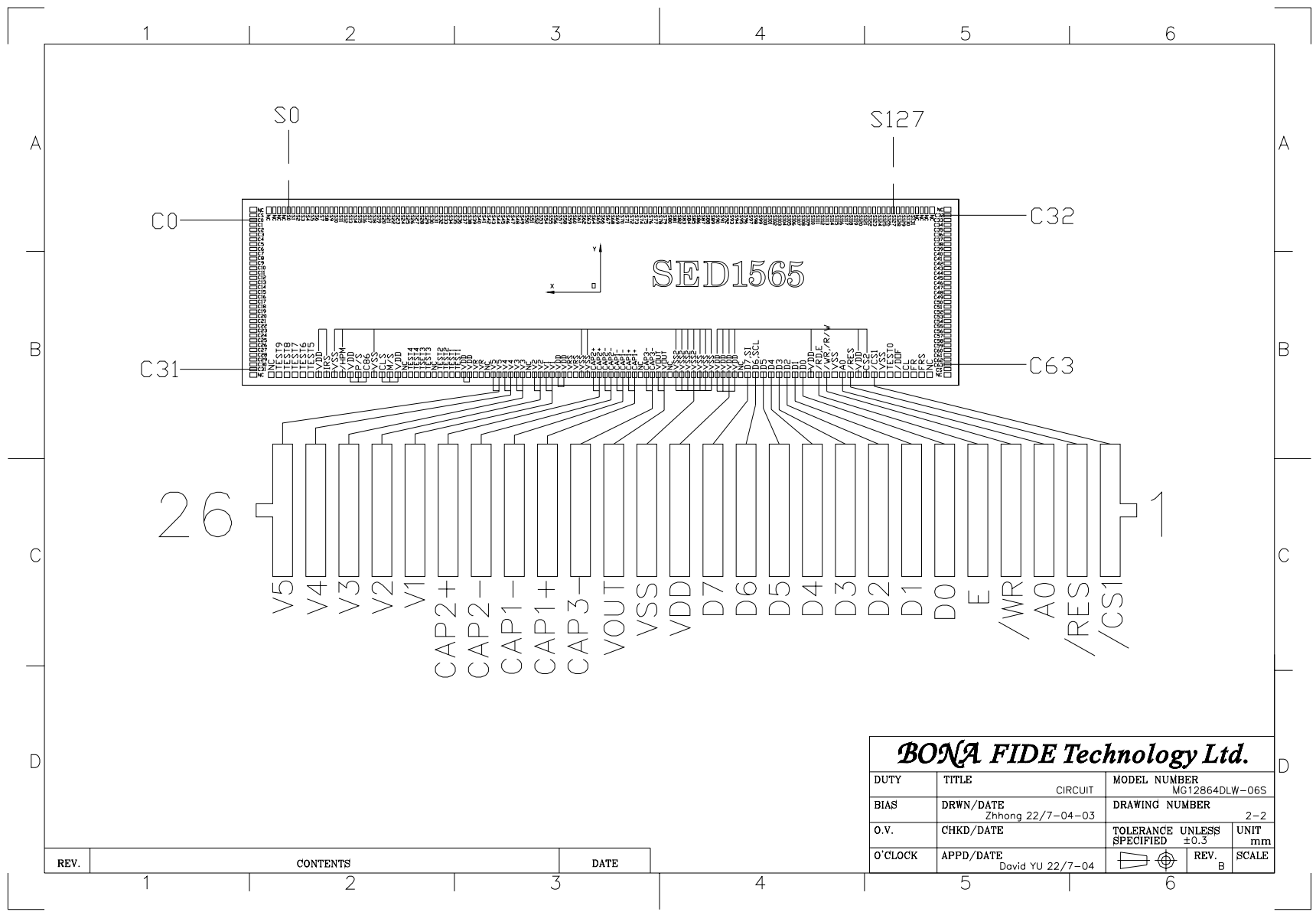


<b>BONA FIDE Technology Ltd.</b>			
DUTY	TITLE	MODEL NUMBER	
	ASSEMBLY SKETCH MAP	MG12864DLW-06S	
BIAS	DRWN/DATE	DRAWING NUMBER	
	Zhhong 11/8-04		
O.V.	CHKD/DATE	TOLERANCE UNLESS SPECIFIED	UNIT
		±0.3	mm
O'CLOCK	APPD/DATE	REV.	SCALE
	David YU 11/8-04	0	

REV.	CONTENTS	DATE
1		

# 5. CIRCUIT DIAGRAM



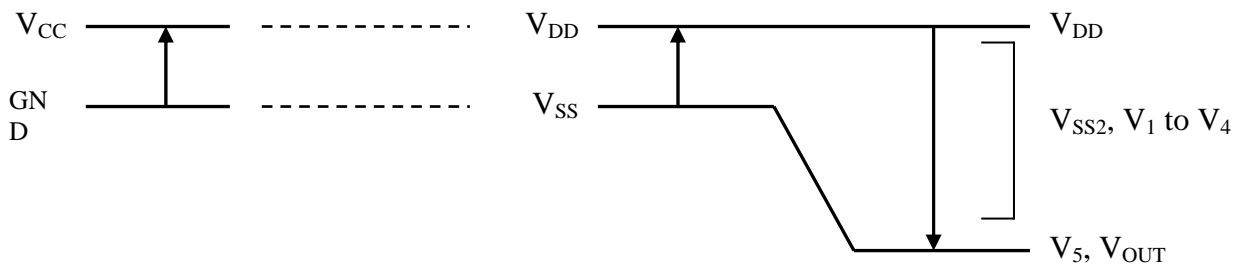


## 6. BLOCK DIAGRAM

13	12	11	10	9	8	7	6	5	4	3	2	1
D7 (SI)	D6 (SCL)	D5	D4	D3	D2	D1	D0	/RD	/WR	A0	/RESET	/CS1
26	25	24	23	22	21	20	19	18	17	16	15	14
V5	V4	V3	V2	V1	CAP2+	CAP2-	CAP1-	CAP1+	CAP3-	VOUT	VSS	VDD

## 7. ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, VSS=0V)

Parameter	Symbol	Conditions	Unite
Power Supply Voltage	V <sub>DD</sub>	-0.3 to +0.7	V
Power supply voltage (2) (VDD standard)	V <sub>SS2</sub>	-0.7 to +0.3	V
With Triple sep-up		-6.0 to +0.3	
With Quad step-up		-4.5 to +0.3	
Power supply voltage (3) (VDD STANDARD)	V <sub>5</sub> , V <sub>OUT</sub>	-18 to +0.3	V
Power supply voltage (4) (VDD STANDARD)	V <sub>1</sub> , V <sub>2</sub> , V <sub>3</sub> , V <sub>4</sub>	V <sub>5</sub> to +0.3	V
Input voltage	V <sub>IN</sub>	-0.3 to V <sub>DD</sub> +0.3	V
Output voltage	V <sub>O</sub>	-0.3 to V <sub>DD</sub> +0.3	V
Operating temperature	T <sub>OPR</sub>	0 °C to 50 °C	°C
Storage temperature	T <sub>STR</sub>	-10 °C to 60 °C	°C



System (MPU) side

SED 1565 Series chip side

### Notes and Cautions:

1. The V<sub>SS2</sub>, V<sub>1</sub> to V<sub>5</sub> and V<sub>OUT</sub> are relative to the V<sub>DD</sub> = 0V reference.
2. Insure that the voltage levels of V<sub>1</sub>, V<sub>2</sub>, V<sub>3</sub> and V<sub>4</sub> are always such that V<sub>DD</sub> ≥ V<sub>1</sub> ≥ V<sub>2</sub> ≥ V<sub>3</sub> ≥ V<sub>4</sub> ≥ V<sub>5</sub>.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings, moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

## 8. DC CHARACTERISTICS

Unless otherwise specified,  $V_{SS}=0V$ ,  $V_{DD}=3.0V\pm 10\%$ ,  $T_a = -40$  to  $85^{\circ}C$

Item	Symbol	condition		Rating			Unit	Applicable Pin
				Min	Typ.	Max		
Operating Voltage(1)	$V_{DD}$			2.7	3.0	3.3	V	$V_{DD}^*1$
Operating Voltage(2)	$V_{SS2}$	(Relative to $V_{DD}$ )		-3.3	-3.0	-2.7	V	$V_{SS2}$
Operating Voltage(3)	Possible Operating Voltage	$V_5$	(Relative to $V_{DD}$ )	-16.0	---	-4.5	V	$V_5^*2$
	Possible Operating Voltage	$V_1, V_2$	(Relative to $V_{DD}$ )	$0.4 \times V_5$	---	$V_{DD}$	V	$V_1, V_2$
	Possible Operating Voltage	$V_3, V_4$	(Relative to $V_{DD}$ )	$V_5$	---	$0.6 \times V_5$	V	$V_3, V_4$
High-level Input Voltage	$V_{IHC}$			$0.8 \times V_{DD}$	---	$V_{DD}$	V	*3
Low-level Input Voltage	$V_{ILC}$			$V_{SS}$	---	$0.2 \times V_{DD}$	V	*3
High-level Output Voltage	$V_{OHC}$	$I_{OH} = -0.5mA$		$0.8 \times V_{DD}$	---	$V_{DD}$	V	*4
Low-level Output Voltage	$V_{OLC}$	$I_{OL} = 0.5mA$		$V_{SS}$	---	$0.2 \times V_{DD}$	V	*4
Input leakage current	$I_{LI}$	$V_{IN} = V_{DD}$ or $V_{SS}$		-1.0	---	1.0	$\mu A$	*5
Output leakage current	$I_{LO}$			-3.0	---	3.0	$\mu A$	*6
Liquid Crystal Driver ON Resistance	$R_{ON}$	$T_a = 25^{\circ}C$ (Relative To $V_{DD}$ )	$V_5 = -14.0V$	---	2.0	3.5	$K\Omega$	SEGN
			$V_5 = -8.0V$	---	3.2	5.4	$K\Omega$	COMn*7
Static Consumption Current	$I_{SSQ}$	$V_5 = -18.0V$ (Relative To $V_{DD}$ )		---	0.01	5	$\mu A$	$V_{SS}, V_{SS2}$
Output Leakage Current	$I_{SO}$			---	0.01	15	$\mu A$	$V_5$
Input Terminal Capacitance	$C_{IN}$	$T_a = 25^{\circ}C$ $f = 1$ MHz		---	5.0	8.0	pF	
Oscillator Frequency	Internal Oscillator	$f_{OSC}$	$T_a = 25^{\circ}C$	18	22	26	KHz	*8
	External Input	$f_{CL}$	SED1565**/1567**	18	22	26	KHz	CL
Internal power	Input voltage	$V_{SS2}$	With Triple (Relative To $V_{DD}$ )	-6.0	---	-1.8	V	$V_{SS2}$
		$V_{SS2}$	With Quad (Relative To $V_{DD}$ )	-4.5	---	-1.8	V	$V_{SS2}$
	Supply Step-up output Voltage Circuit	$V_{OUT}$	(Relative To $V_{DD}$ )	-18.0	---	---	V	$V_{OUT}$
	Voltage regulator Circuit Operating voltage	$V_{OUT}$	(Relative To $V_{DD}$ )	-18.0	---	-6.0	V	$V_{OUT}$
	Voltage follower Circuit Operating voltage	$V_5$	(Relative To $V_{DD}$ )	-16.0	---	-4.5	V	$V_5^*9$
Base voltage	$V_{REG0}$	$T_a = 25^{\circ}C$	-0.05%/°C	-2.16	-2.10	-2.04	V	*10
	$V_{REG1}$	(Relative To $V_{DD}$ )	-0.2%/°C	-5.15	-4.9	-4.65	V	*10

- Dynamic Consumption Current (1), During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used.

**T<sub>a</sub> = 25°C**

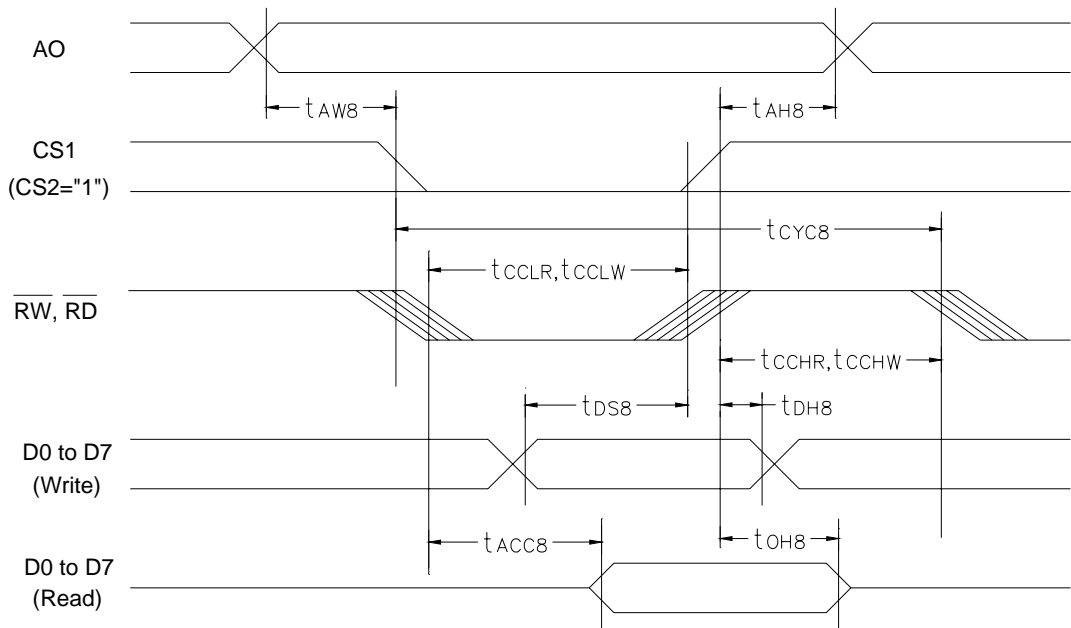
Item	Symbol	Condition	Rating			Units	Notes
			Min	Typ.	Max		
<b>Display Pattern OFF</b>	IDD (1)	V <sub>DD</sub> = 3.0V, V <sub>5</sub> -V <sub>DD</sub> = -11.0V	---	16	27	μA	*11
<b>Display Pattern Checker</b>	IDD (1)	V <sub>DD</sub> = 3.0V, V <sub>5</sub> -V <sub>DD</sub> = -11.0V	---	21	35	μA	*11

- Dynamic Consumption Current (2), During Display, with the Internal Power Supply ON

Item	Symbol	Condition		Rating			Units	Notes
				Min	Typ.	Max		
<b>Display Pattern OFF</b>	IDD (2)	V <sub>DD</sub> = 3.0V, Quad step-up voltage. V <sub>5</sub> -V <sub>DD</sub> = -11.0V	Normal Mode	---	81	135	μA	*12

## 9. TIMING CHARACTERISTICS

### 9-1. System Bus Read/Write Characteristics 1 (for the 8080 Series MPU)



( $V_{DD} = 4.5V$  to  $5.5V$ ,  $T_a = -40$  to  $85^\circ C$ )

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	AO	$t_{AH8}$	---	0	---	ns
Address setup time	AO	$t_{AW8}$	---	0	---	ns
System cycle time	AO	$t_{CYC8}$	---	166	---	ns
Control L pulse width $\overline{WR}$	$\overline{WR}$	$t_{CCLW}$	---	30	---	ns
Control L pulse width $\overline{RD}$	$\overline{RD}$	$t_{CCLR}$	---	70	---	ns
Control H pulse width $\overline{WR}$	$\overline{WR}$	$t_{CCHW}$	---	30	---	ns
Control H pulse width $\overline{RD}$	$\overline{RD}$	$t_{CCHR}$	---	30	---	ns
Data setup time	D0 to D7	$t_{DS8}$	---	30	---	ns
Address hold time		$t_{DH8}$	---	10	---	ns
$\overline{RD}$ access time	D0 to D7	$t_{ACC8}$	$C_L = 100$ pF	---	70	ns
Output disable time		$t_{OH8}$	---	5	50	ns

( $V_{DD} = 2.7V$  to  $4.5V$ ,  $T_a = -40$  to  $85^\circ C$ )

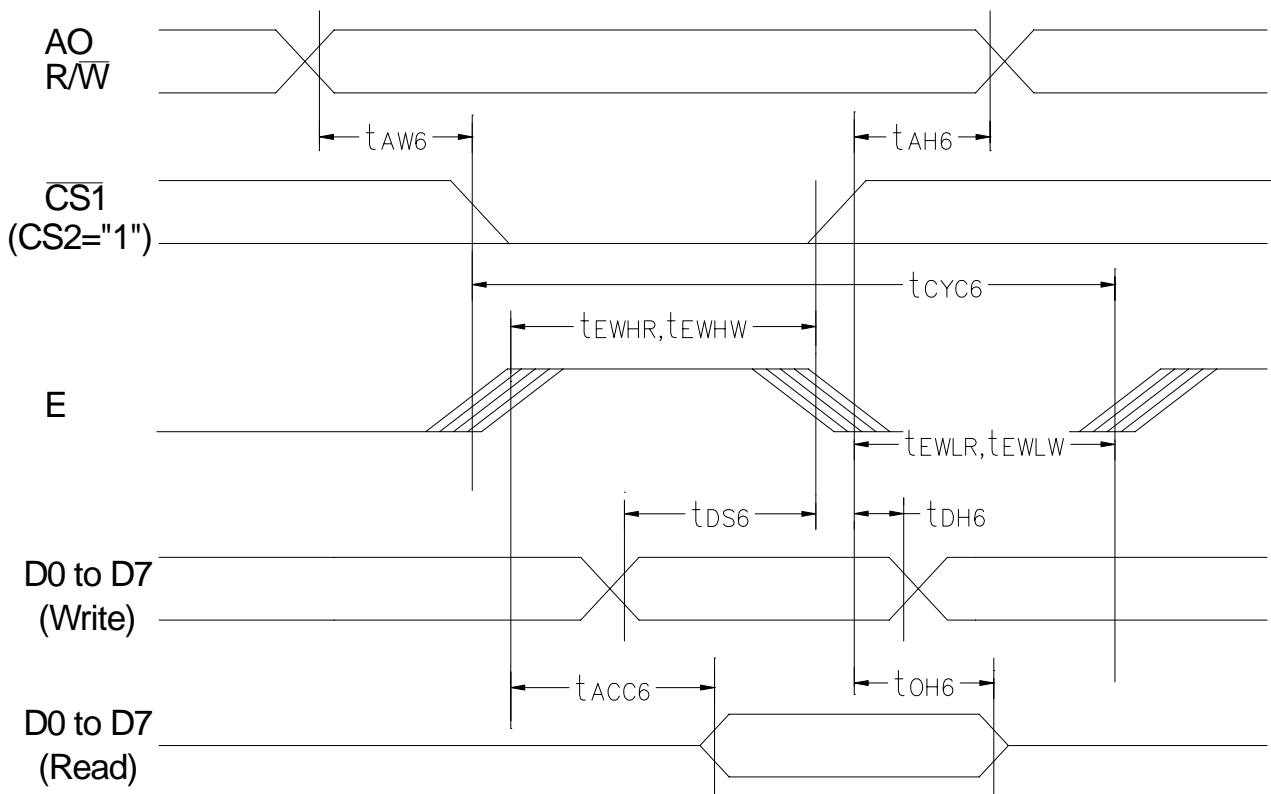
Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	AO	$t_{AH8}$	---	0	---	ns
Address setup time	AO	$t_{AW8}$	---	0	---	ns
System cycle time	AO	$t_{CYC8}$	---	300	---	ns
Control L pulse width $\overline{WR}$	$\overline{WR}$	$t_{CCLW}$	---	60	---	ns
Control L pulse width $\overline{RD}$	$\overline{RD}$	$t_{CCLR}$	---	120	---	ns
Control H pulse width $\overline{WR}$	$\overline{WR}$	$t_{CCHW}$	---	60	---	ns
Control H pulse width $\overline{RD}$	$\overline{RD}$	$t_{CCHR}$	---	60	---	ns
Data setup time	D0 to D7	$t_{DS8}$	---	40	---	ns
Address hold time		$t_{DH8}$	---	15	---	ns
$\overline{RD}$ access time	D0 to D7	$t_{ACC8}$	$C_L = 100$ pF	---	140	ns
Output disable time		$t_{OH8}$	---	10	100	ns

( $V_{DD} = 1.8V$  to  $2.7V$ ,  $T_a = -40$  to  $85^{\circ}C$ )

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	AO	$t_{AH8}$	---	0	---	ns
Address setup time	AO	$t_{AW8}$	---	0	---	ns
System cycle time	AO	$t_{CYC8}$	---	1000	---	ns
Control L pulse width $\overline{WR}$	$\overline{WR}$	$t_{CCLW}$	---	120	---	ns
Control L pulse width $\overline{RD}$	$\overline{RD}$	$t_{CCLR}$	---	240	---	ns
Control H pulse width $\overline{WR}$	$\overline{WR}$	$t_{CCHW}$	---	120	---	ns
Control H pulse width $\overline{RD}$	$\overline{RD}$	$t_{CCHR}$	---	120	---	ns
Data setup time	D0 to D7	$t_{DS8}$	---	80	---	ns
Address hold time		$t_{DH8}$	---	30	---	ns
$\overline{RD}$ access time		$t_{ACC8}$	$C_L = 100$ pF	---	280	ns
Output disable time		$t_{OH8}$		10	200	ns

- \*1. The input signal rise time and fall time ( $t_r$ ,  $t_f$ ) is specified at 15 ns or less. When the system cycle time is extremely fast,  $(t_r + t_f) \leq (t_{CYC8} - t_{CCLW} - t_{CCHW})$  for  $(t_r + t_f) \leq (t_{CYC8} - t_{CCLR} - t_{CCHR})$  are specified.
- \*2. All timing is specified using 20% and 80% of  $V_{DD}$  as the reference.
- \*3.  $t_{CCLW}$  and  $t_{CCLR}$  are specified as the overlap between  $\overline{CS1}$  being "L" ( $CS2 = "H"$ ) and  $\overline{WR}$  and  $\overline{RD}$  being at the "L" level.

## 9-2. System Bus Read/Write Characteristics 2 (6800 Series MPU)



( $V_{DD} = 4.5V$  to  $5.5V$ ,  $T_a = -40$  to  $85^{\circ}C$ )

Item	Signal	Symbol	Condition	Rating		Units	
				Min	Max		
Address hold time	AO	$t_{AH6}$	---	0	---	ns	
Address setup time		$t_{AW6}$	---	0	---	ns	
System cycle time	AO	$t_{CYC6}$	---	166	---	ns	
Data setup time	Do to D7	$t_{DS6}$	---	30	---	ns	
Data hold time		$t_{DH6}$	---	10	---	ns	
Access time		$t_{ACC6}$	Cl = 100pF	---	70	ns	
Output disable time		$t_{OH6}$		---	10	50	ns
Enable H pulse time	Read	E		---	70	---	ns
	Write						
Enable L pulse time	Read	E		---	30	---	ns
	Write						
Enable H pulse time	Read	E		---	70	---	ns
	Write						
Enable L pulse time	Read	E		---	30	---	ns
	Write						

( $V_{DD} = 2.7V$  to  $4.5V$ ,  $T_a = -40$  to  $85^{\circ}C$ )

Item	Signal	Symbol	Condition	Rating		Units	
				Min	Max		
Address hold time	AO	$t_{AH6}$	---	0	---	ns	
Address setup time		$t_{AW6}$	---	0	---	ns	
System cycle time	AO	$t_{CYC6}$	---	300	---	ns	
Data setup time	D0 to D7	$t_{DS6}$	---	40	---	ns	
Data hold time		$t_{DH6}$	---	15	---	ns	
Access time		$t_{ACC6}$	$C_L = 100pF$	---	140	ns	
Output disable time		$t_{OH6}$		---	10	100	ns
Enable H pulse time	Read	E		---	120	---	ns
	Write						
Enable L pulse time	Read	E		---	60	---	ns
	Write						
Enable H pulse time	Read	E		---	60	---	ns
	Write						
Enable L pulse time	Read	E		---	60	---	ns
	Write						

( $V_{DD} = 1.8V$  to  $2.7V$ ,  $T_a = -40$  to  $85^{\circ}C$ )

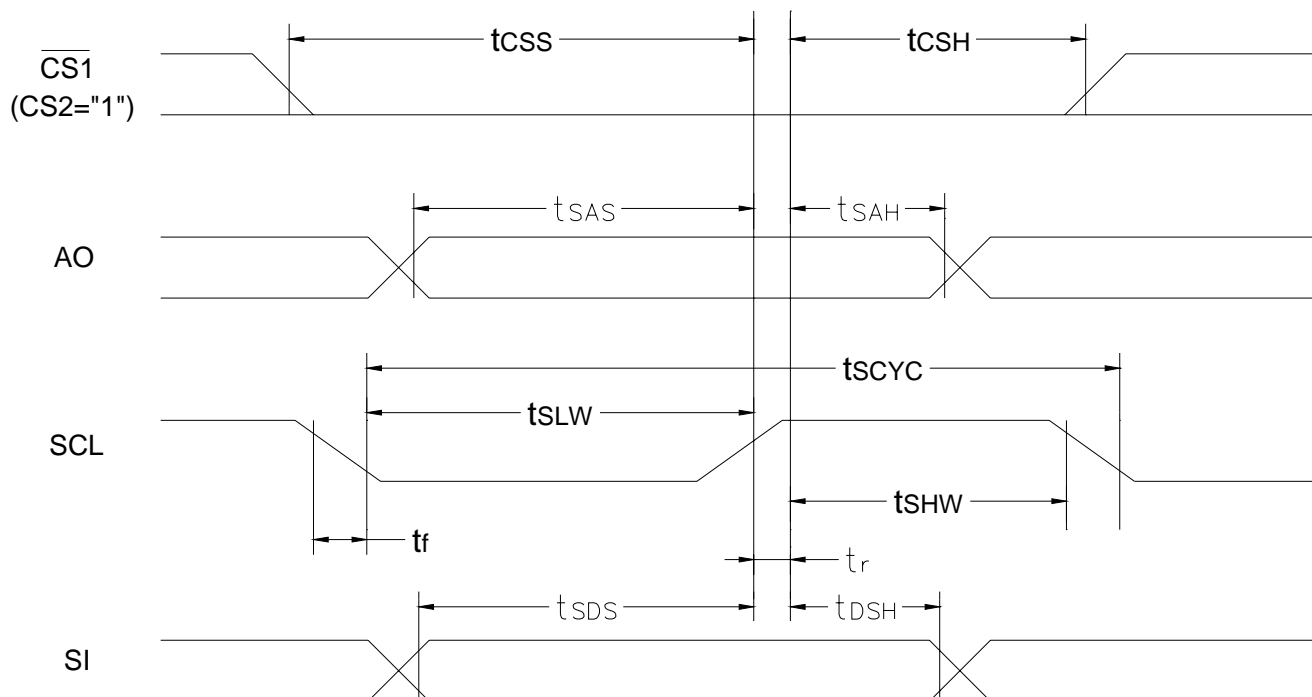
Item	Signal	Symbol	Condition	Rating		Units	
				Min	Max		
Address hold time	AO	$t_{AH6}$	---	0	---	ns	
Address setup time		$t_{AW6}$	---	0	---	ns	
System cycle time	AO	$t_{CYC6}$	---	1000	---	ns	
Data setup time	D0 to D7	$t_{DS6}$	---	80	---	ns	
Data hold time		$t_{DH6}$	---	30	---	ns	
Access time		$t_{ACC6}$	$C_L = 100pF$	---	280	ns	
Output disable time		$t_{OH6}$		---	10	200	ns
Enable H pulse time	Read	E		---	240	---	ns
	Write						
Enable L pulse time	Read	E		---	120	---	ns
	Write						
Enable H pulse time	Read	E		---	120	---	ns
	Write						
Enable L pulse time	Read	E		---	120	---	ns
	Write						

\*1. The input signal rise time and fall time ( $t_r$ ,  $t_f$ ) is specified at 15 ns or less. When the system cycle time is extremely fast,  $(t_r + t_f) \leq (t_{CYC6} - t_{EWLW} - t_{EWHW})$  for  $(t_r + t_f) \leq (t_{CYC6} - t_{EWLR} - t_{EWHR})$  are specified.

\*2. All timing is specified using 20% and 80% of  $V_{DD}$  as the reference.

\*3.  $t_{EWLW}$  and  $t_{EWLR}$  are specified as the overlap between  $\overline{CS1}$  being "L" ( $CS2 = "H"$ ) and E.

### 9-3.Serial Interface



( $V_{DD} = 4.5V$  to  $5.5V$ ,  $T_a = -40$  to  $85^{\circ}C$ )

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Serial clock period	SCL	$t_{SCYC}$	---	200	---	ns
SCL"H" pulse width		$t_{SHW}$	---	75	---	ns
SCL"L" pulse width		$t_{SLW}$	---	75	---	ns
Address setup time	AO	$t_{SAS}$	---	50	---	ns
Address hold time		$t_{SAH}$	---	100	---	ns
Data setup time	SI	$t_{SDS}$	---	50	---	ns
Data hold time		$t_{SDH}$	---	50	---	ns
CS-SCL time	CS	$t_{CSS}$	---	100	---	ns
		$t_{CSH}$	---	100	---	ns

( $V_{DD} = 2.7V$  to  $4.5V$ ,  $T_a = -40$  to  $85^{\circ}C$ )

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Serial clock period	SCL	$t_{SCYC}$	---	250	---	ns
SCL"H" pulse width		$t_{SHW}$	---	100	---	ns
SCL"L" pulse width		$t_{SLW}$	---	100	---	ns
Address setup time	AO	$t_{SAS}$	---	150	---	ns
Address hold time		$t_{SAH}$	---	150	---	ns
Data setup time	SI	$t_{SDS}$	---	100	---	ns
Data hold time		$t_{SDH}$	---	100	---	ns
CS-SCL time	CS	$t_{CSS}$	---	150	---	ns
		$t_{CSH}$	---	150	---	ns

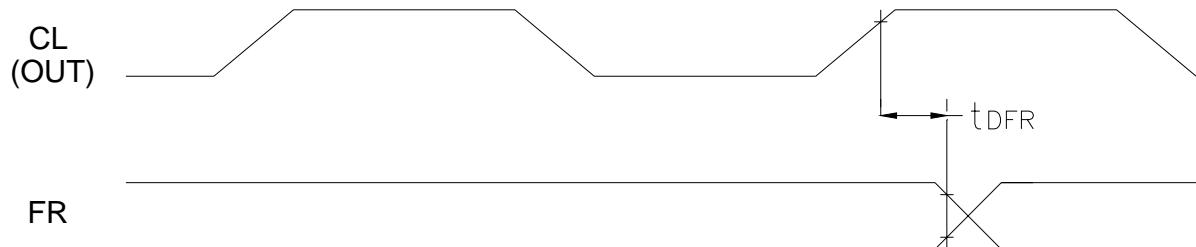
( $V_{DD} = 1.8V$  to  $2.7V$ ,  $T_a = -40$  to  $85^{\circ}C$ )

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Serial clock period	SCL	$t_{SCYC}$	---	400	---	ns
SCL"H" pulse width		$t_{SHW}$	---	150	---	ns
SCL"L" pulse width		$t_{SLW}$	---	150	---	ns
Address setup time	AO	$t_{SAS}$	---	250	---	ns
Address hold time		$t_{SAH}$	---	250	---	ns
Data setup time	SI	$t_{SDS}$	---	150	---	ns
Data hold time		$t_{SDH}$	---	150	---	ns
CS-SCL time	CS	$t_{CSS}$	---	250	---	ns
		$t_{CSH}$	---	250	---	ns

\*1. The input signal rise and fall time ( $t_r$ ,  $t_f$ ) are specified at 15 ns or less.

\*2. All timing is specified using 20% and 80% of  $V_{DD}$  as the standard.

#### 9-4. Display control output timing



( $V_{DD} = 4.5V$  to  $5.5V$ ,  $T_a = -40$  to  $85^{\circ}C$ )

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time	FR	$t_{DFR}$	$C_L = 50$ pF	---	10	40	ns

( $V_{DD} = 2.7$  V to  $4.5V$ ,  $T_a = -40$  to  $85^{\circ}C$ )

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time	FR	$t_{DFR}$	$C_L = 50$ pF	---	20	80	ns

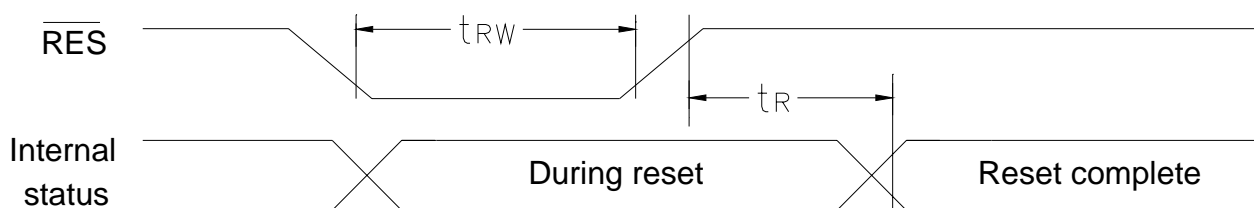
( $V_{DD} = 1.8$  V to  $2.7$  V,  $T_a = -40$  to  $85^{\circ}C$ )

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time	FR	$t_{DFR}$	$C_L = 50$ pF	---	50	200	ns

\*1. Valid only when the master mode is selected.

\*2. All timing is based on 20% and 80% of  $V_{DD}$ .

## 9-5.Reset Timing



( $V_{DD} = 4.5V$  to  $5.5V$ ,  $T_a = -40$  to  $85^{\circ}C$ )

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time		$t_R$	---	---	---	0.5	$\mu s$
Reset "L" pulse width	RES	$t_{RW}$		0.5	---	---	$\mu s$

( $V_{DD} = 2.7V$  to  $4.5V$ ,  $T_a = -40$  to  $85^{\circ}C$ )

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time		$t_R$	---	---	---	1.0	$\mu s$
Reset "L" pulse width	RES	$t_{RW}$		1.0	---	---	$\mu s$

( $V_{DD} = 1.8 V$  to  $2.7 V$ ,  $T_a = -40$  to  $85^{\circ}C$ )

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time		$t_R$	---	---	---	1.5	$\mu s$
Reset "L" pulse width	RES	$t_{RW}$		1.5	---	---	$\mu s$

\*1. All timing is specified with 20% and 80% of  $V_{DD}$  as the standard.

# 10. REFERENCE CIRCUIT EXAMPLES

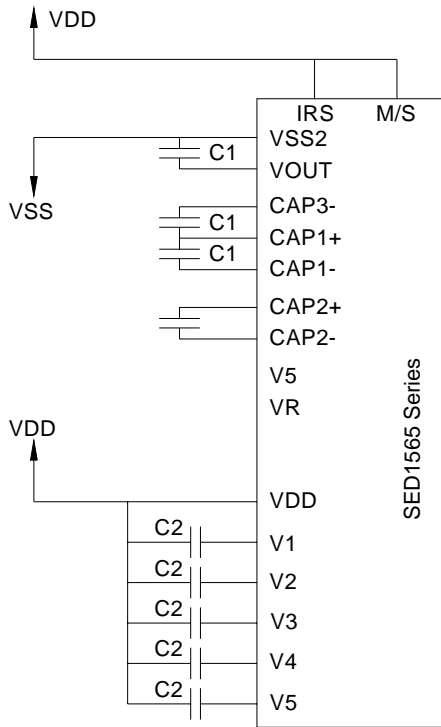
## Reference Circuit Examples

Figures shows reference circuit examples.

- When user all of the set-up circuit, voltage regulating circuit and V/F circuit.

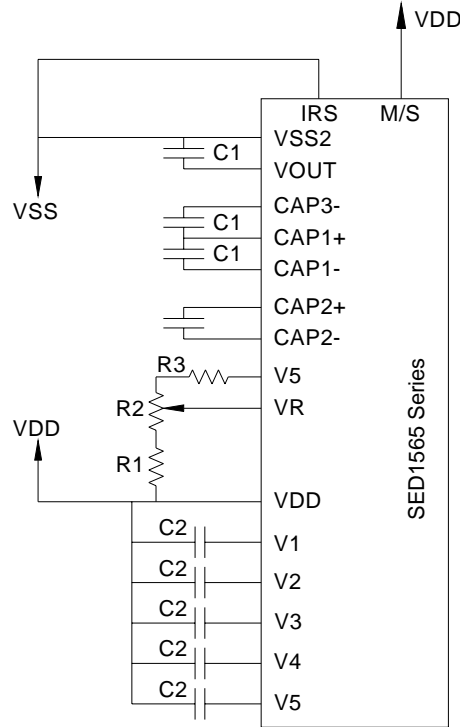
1. When the voltage regulator internal resistor is used.

(Example where  $V_{SS2} = V_{SS}$ , with 4 x step\_up)



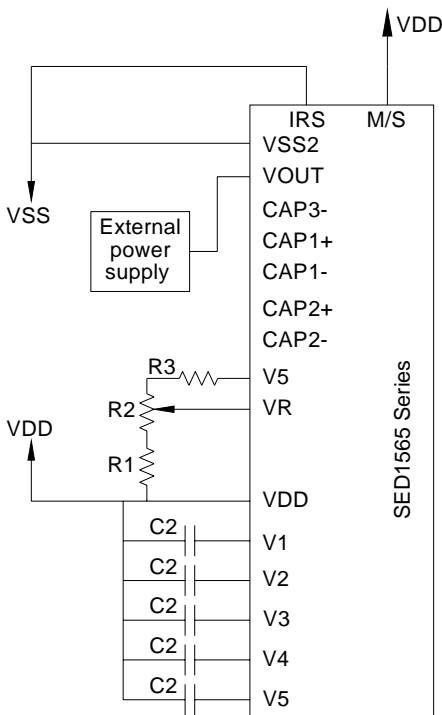
1. When the voltage regulator internal resistor is not used.

(Example where  $V_{SS2} = V_{SS}$ , with 4 x step\_up)

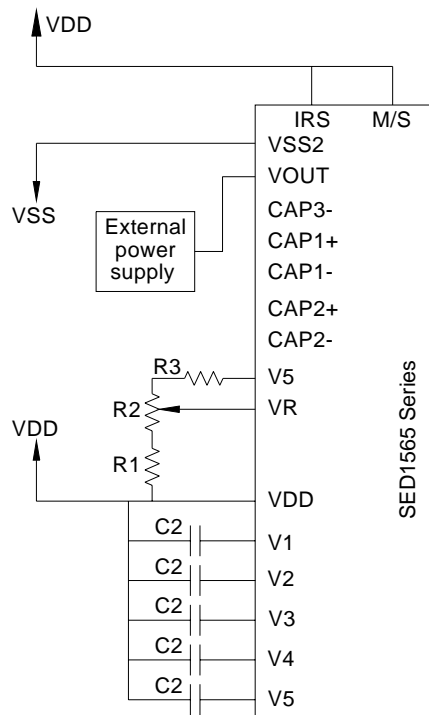


- When the voltage regulator circuit and V/F circuit alone are used

1. When the V5 voltage regulator internal resistor is not used.



1. When the V5 voltage regulator internal resistor is not used.



## 11. INTERFACE PIN CONNECTIONS

Pin No.	Symbol	Level	Description
1	/CS1	H-L	Chip select signal
2	/RESET	H-L	Reset
3	A0	H/L	H: D0-D7 are display data, L: D0-D7 are control data
4	/WR	H-L	8080: active LOW, 6060: H -> read, L -> write
5	/RD	H-L	8080: active LOW, 6060: HIGH
6	D0	H/L	Parallel data input
7	D1	H/L	Parallel data input
8	D2	H/L	Parallel data input
9	D3	H/L	Parallel data input
10	D4	H/L	Parallel data input
11	D5	H/L	Parallel data input
12	D6	H/L	Parallel data input
13	D7	H/L	Parallel data input
14	VDD	---	Power supply
15	VSS	---	Power supply
16	VOUT	---	DC/DC voltage converter
17	CAP3-	---	DC/DC voltage converter
18	CAP1+	---	DC/DC voltage converter
19	CAP1-	---	DC/DC voltage converter
20	CAP2-	---	DC/DC voltage converter
21	CAP2+	---	DC/DC voltage converter
22	V1	---	LCD operating voltage
23	V2	---	LCD operating voltage
24	V3	---	LCD operating voltage
25	V4	---	LCD operating voltage
26	V5	---	LCD operating voltage

Capacitance value for boosting should be more than 1.0uF.

## 12. PART LIST

ITEM	DESCRIPTION	QTY.	UNITE
1	LCD PANEL, SIZE 77.5x(51.3+44.8)X1.1mm, STN Y/G TRANSFLECTIVE, 6:00, WIDE TEMP.	1	PCS
2	IC, SED1565	1	PCS
3	FPC, L72.0 x W13.5mm, PITCH0.5mm, 26PINS	1	PCS
4	SILICON	---	PCS
5	“T” TAPE, BLACK TAPE, SINGLE SIDE ADHESIVE	2	PCS
6	“SONY” DOUBLE SIDE TAPE,	12	PCS
7	DIFFUSER	1	PCS
8	REFLECTOR	1	PCS
9	PLASTIC GUIDE	1	PCS
10	PCB	1	PCS
11	LED DIES, Y/G COLOR	16	PCS
12	LEAD WIRE, RED COLOR AND BLACK COLOR WITH SOCKET	1	SET
13	LOT No label, Size: 34x5.0mm, material :plain paper, Font type: MS PGothic, Text height:1.4mm	1	PCS
14	Made in China label, Size: 34x5.3mm, material: plain paper, Font type: Book Antiqua, Text height: 2mm	1	PCS
15	QC pass label, Size: 13.2x9.2 ellipse, material: plain paper, Font type: Arial, Text height: 2mm	1	PCS

### 13. DESCRIPTION OF INTERNAL PIN CONNECTION & FUNCTION SET

Class.	Symbol	Level	Description
H/W	IRS	HIGH	Use the internal resistors
	HPM	LOW	High power mode
	P/S	LOW	Parallel data input
	C86	LOW	8080 MPU interface
	CLS	HIGH	Internal oscillator circuit is enable
S/W	ADC	LOW	ADC select (SEG0 -> SEG128)
	D3	HIGH	Common output mode select ( COM63 -> COM0 )

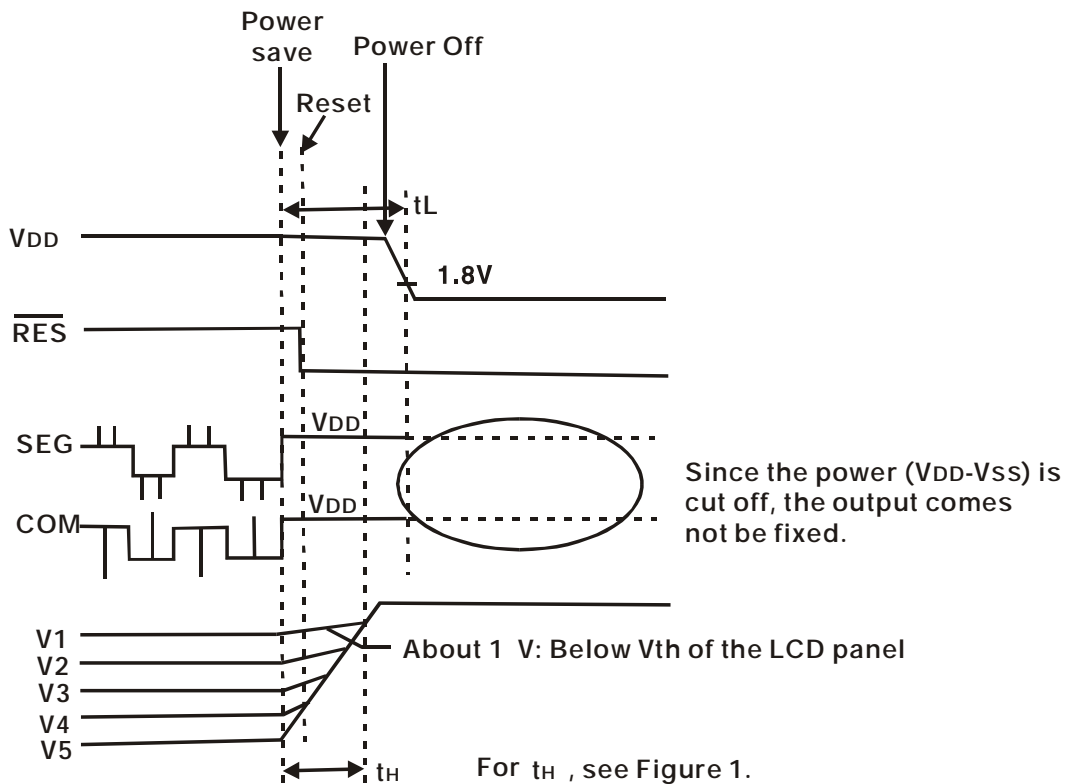
### 14. PRECAUTIONS ON TURNING OFF THE POWER

In case of SED1565DBB, SED1566DBB, SED1567DBB, SED1568DBB,  
Observe Paragraph 1 as the basic rule.

<Turning the power (VDD – VSS) off>

1) Power Save (The LCD powers (VDD – V5) are off.) -> Power (VDD – VSS) OFF

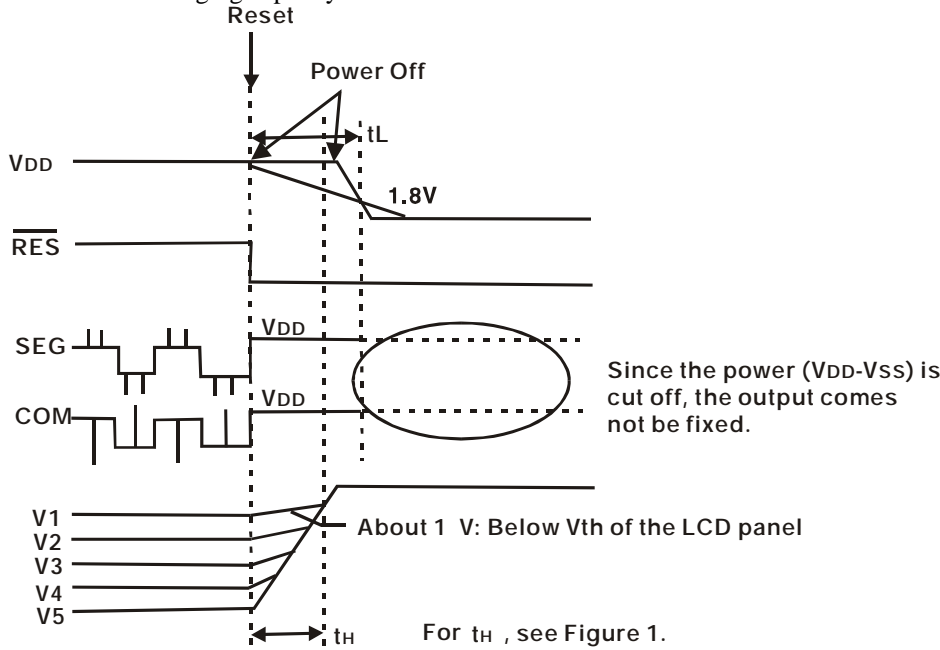
- observe  $t_L > t_H$
- When  $t_L < t_H$ , an irregular display may occur.  
Set  $t_L$  on the MPU according to the software.  $t_H$  is determined according to the external capacity C2 (smoothing capacity of V5 ~ V1) and the driver's discharging capacity.



<Turning the power (VDD - VSS) off: When command control is not possible.>

2) Reset (The LCD powers (VDD - VSS) are off.) -> Power (VDD - VSS) OFF

- Observe  $t_L > t_H$
- When  $t_L < t_H$ , an irregular display may occur.
- For  $t_L$ , make the power (VDD - VSS) falling characteristics longer or consider any other method.  $t_H$  is determined according to the external capacity  $C_2$  (smoothing capacity of V5 to V1) and the driver's discharging capacity.



<Reference Data>

V5 voltage falling (discharge) time ( $t_H$ ) after the process of operation -> power save -> reset.

V5 voltage falling (discharge) time ( $t_H$ ) after the process of operation -> reset.

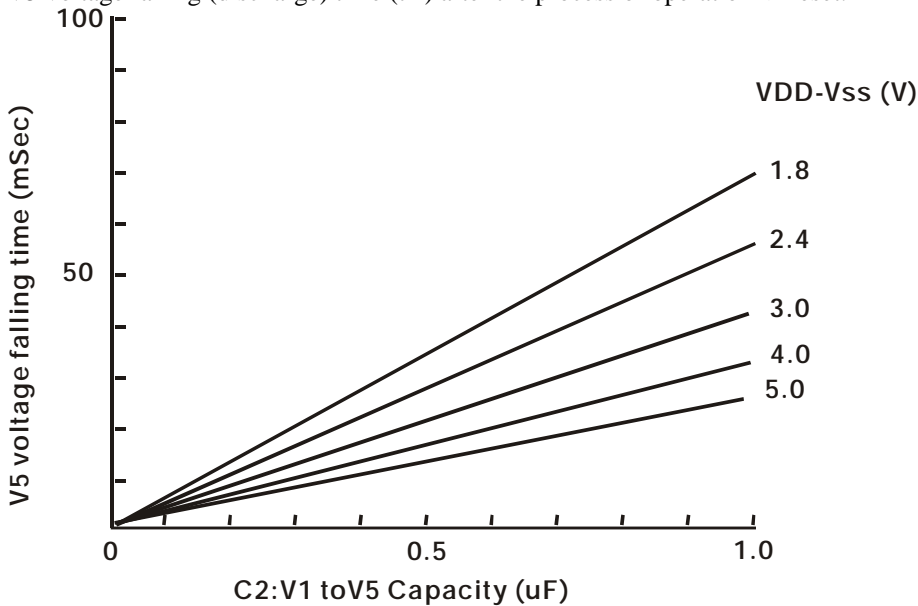


Figure 1

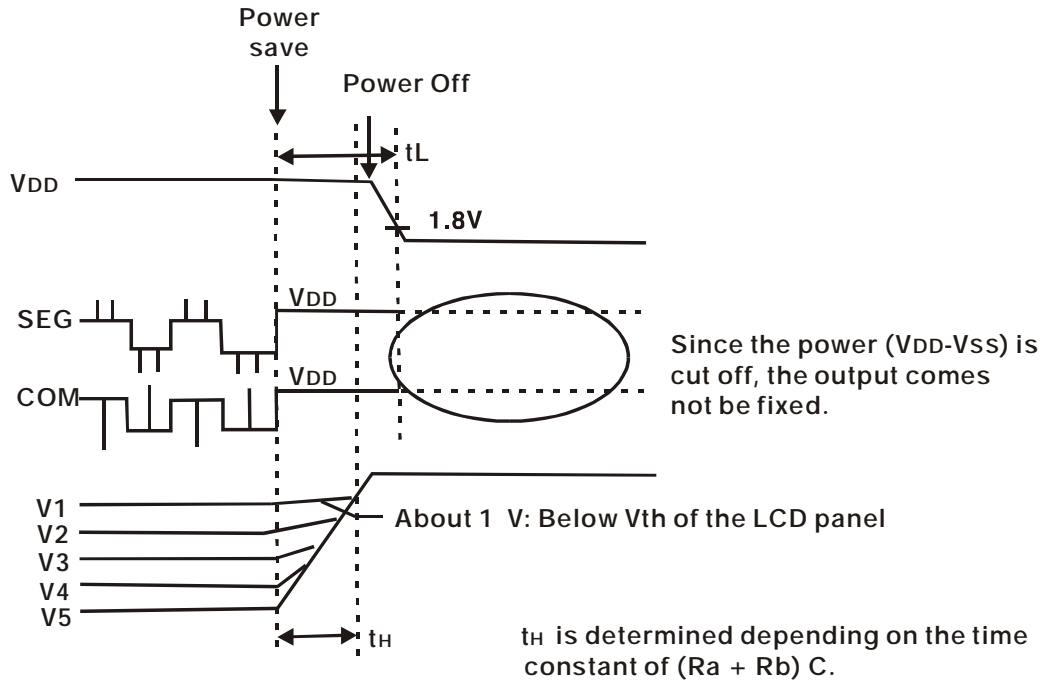
In case of other models than the above

<Turning the power (VDD – VSS) off>

Power save (The LCD powers (VDD – VSS) are off.) -> Power (VDD – VSS) OFF

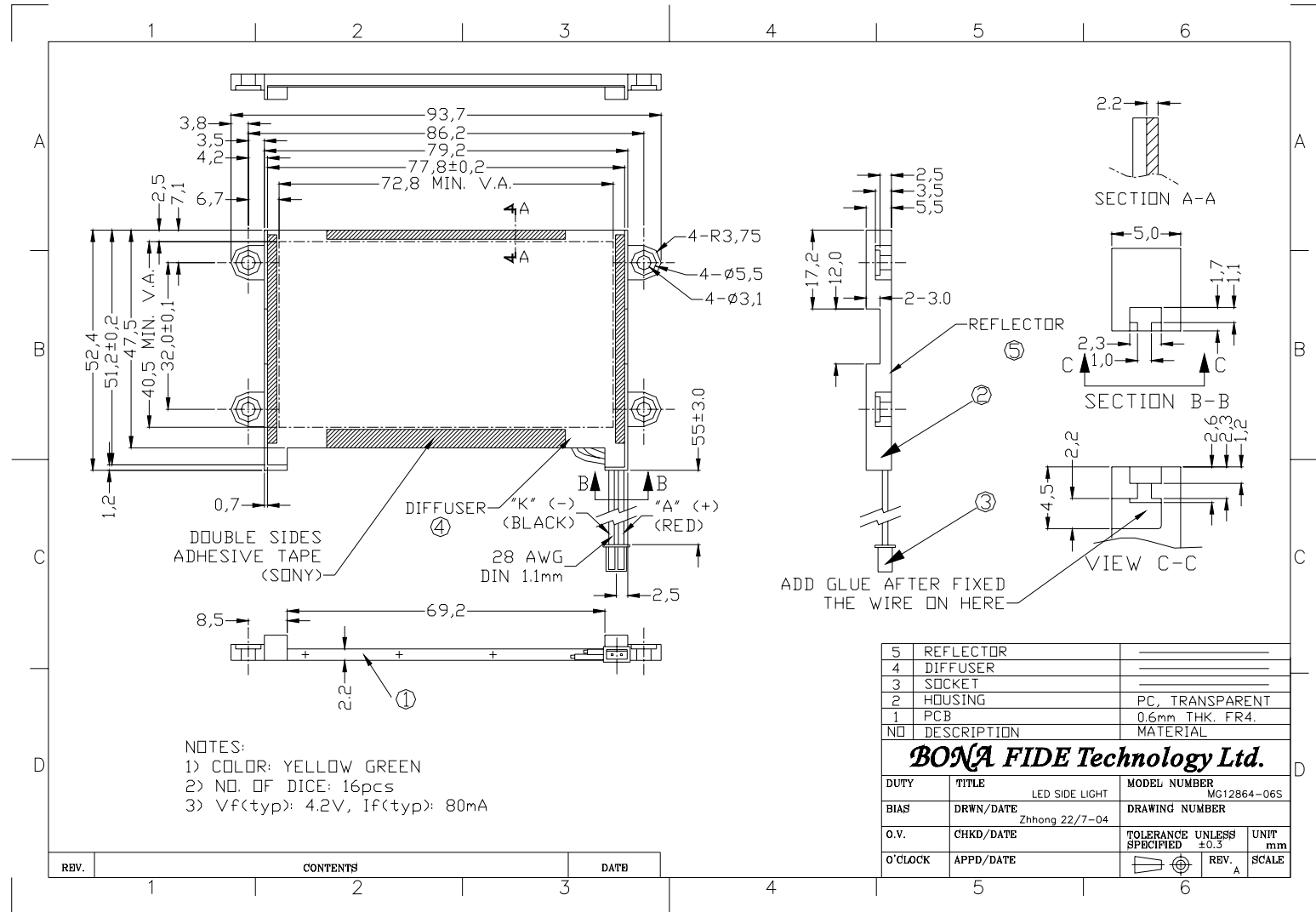
- Observe  $t_L > t_H$ .
- When  $t_L < t_H$ , an irregular display may occur.

Set  $t_L$  on the MPU according to the software,  $t_H$  is determined according to the external capacity C (smoothing capacity of V5 to V!) and the external resistors  $R_a + R_b$  (for V5 voltage regulation)



# 15. DETAIL SPECIFICATIONS OF BACK LIGHT

## a) Outline Dimensions



## b) Mechanical Specifications

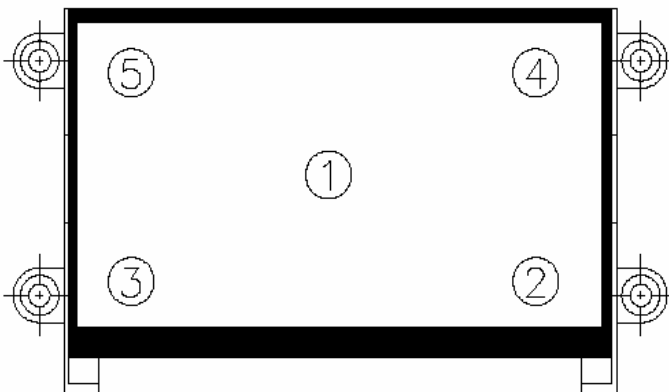
ITEM	NOMINAL DIMENSIONS	UNIT
OUTLINE SIZE(L x W x H)	93.7 x 52.4 x 5.5	mm
VIEWING AREA(L x W)	72.8 x 40.5	mm
CONTACT PIN PITCH/LENGTH	NIL	mm
NO. OF LED DICE	16	---

## c) Electrical/Optical Characteristics (Ta=25°C, If=80mA typ.)

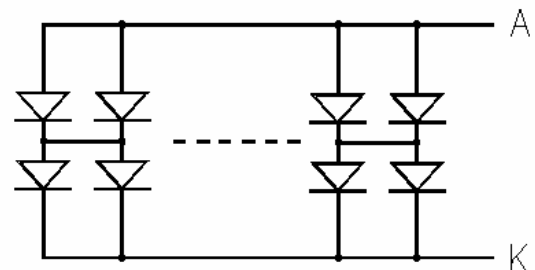
MODE	PARAMETER	UNIT
COLOR	YELLOW GREEN	---
WAVE LENGTH ( )	568	nm
AVERAGE LUMINOUS INTENSITY (Iv)	32.09	Cd/m <sup>2</sup>
FORWARD VOLTAGE (Vf)	4.2 typ	---

## d) Absolute Maximum Rating

FORWARD CURRENT	120mA	If
REVERSE VOLTAGE	5V	Vr
POWER DISSIPATION	504mW	Pd
OPERATING TEMPERATURE	-20°C TO 70°C	Top
STORAGE TEMPERATURE	-30°C TO 80°C	Tstg



TESTING POINT



CIRCUIT DIAGRAM

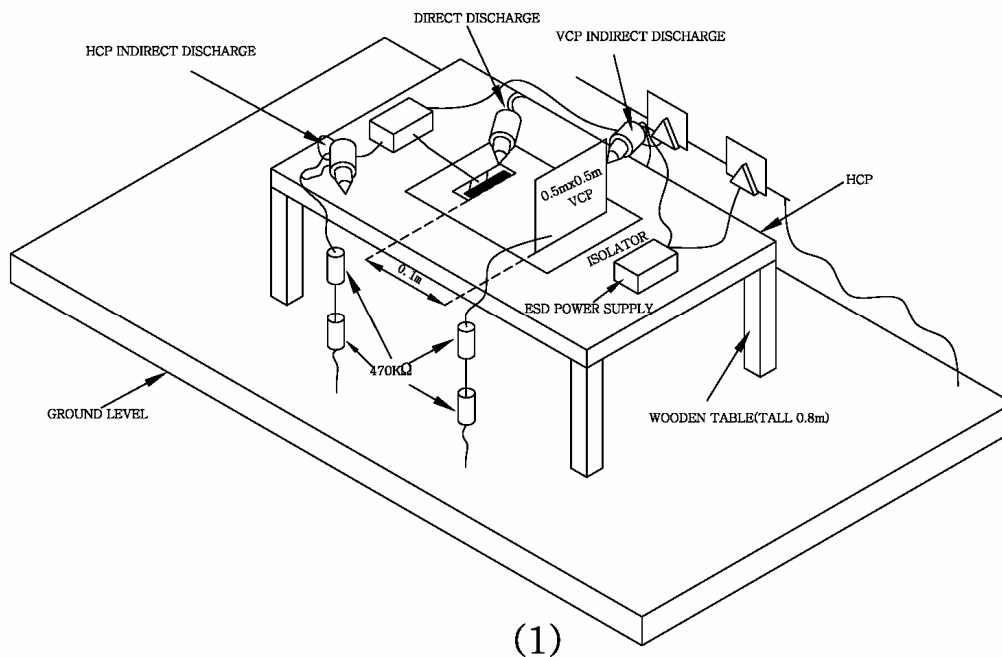
### REMARK:

1. AVERAGE LUMINOUS INTENSITY IS THE AVERAGE VALUE OF THE FIVE INDICATED POINTS AS SHOWN.
2. MEASUREMENT INSTRUMENT: BM-7, APERTURE: 10mm.

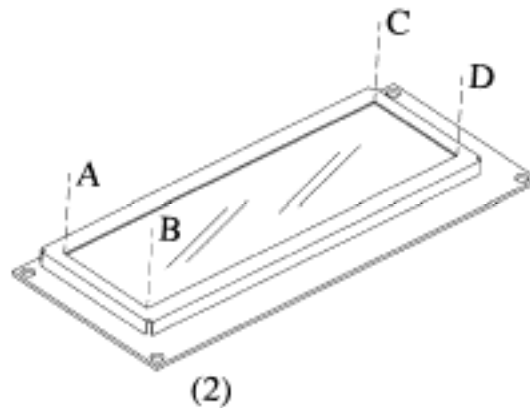
## 16. ELECTRO-STATIC DISCHARGE MAXIMUM RATING (OPTION)

Item	Description	
Testing environment	Ambient temperature: 15°C to 35°C Humidity: 30% to 60% LCM (E.U.T): Power up	
Testing equipment	Manufacture: Noise Ken, Model No. ESD-100L	
Testing condition	See drawing 1	
Direct discharge	0 to +/-6 KV	Discharge point, see drawing 2
Indirect discharge	0 to +/-12KV	Discharge point, see drawing 1
Pass condition	No malfunction of unit. Temporary malfunction of unite which can be recovered by system reset.	
Fail condition	No-recoverable malfunction of LCM or system.	

**Fig. 1: ESD Testing Equipment:**



**Fig. 2: Direct Contact Discharge**  
Contact point: A.B.C.D



## 17. RELIABILITY

### 17-1. Content of Reliability Test

Environmental Test				
No.	Test Item	Content of Test	Test Condition	Applicable Standard
1	High temperature storage	Endurance test applying the high storage temperature for a long time.	60 °C 200 hrs	-----
2	Low temperature storage	Endurance test applying the low storage temperature for a long time.	-10 °C 200 hrs	-----
3	High temperature operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	50 °C 200 hrs	-----
4	Low temperature operation	Endurance test applying the electric stress under low temperature for a long time.	0 °C 200 hrs	-----
5	High temperature / Humidity storage	Endurance test applying the high temperature and high humidity storage for a long time.	60 °C , 90 %RH 96 hrs	MIL-202E-103B JIS-C5023
6	High temperature / Humidity operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	40 °C , 90 %RH 96 hrs	MIL-202E-103B JIS-C5023
7	Temperature cycle	Endurance test applying the low and high temperature cycle.  $  \begin{array}{ccccc}  -10^{\circ}\text{C} & \rightleftharpoons & 25^{\circ}\text{C} & \rightleftharpoons & 60^{\circ}\text{C} \\  30\text{min} & \leftarrow & 5\text{min.} & \rightarrow & 30\text{min} \\  \longleftarrow & & & & \longrightarrow \\  & & 1 \text{ cycle} & &   \end{array}  $	-----	
Mechanical Test				
8	Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz → 1.5mmp-p 22~500Hz → 1.5G Total 0.5hrs	MIL-202E-201A JIS-C5025 JIS-C7022-A-10
9	Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G half sign wave 11 msdc 3 times of each direction	MIL-202E-213B
10	Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115 mbar 40 hrs	MIL-202E-105C
Others				
11	Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V , RS=1.5 kΩ CS=100 pF 1 time	MIL-883B-3015.1

\*\*\* Supply voltage for logic system = VDD. Supply voltage for LCD system = Operating voltage at 25°C.

### 17-2. Failure Judgment Criterion

Criterion Item	Test Item No.											Failure Judgment Criterion	
	1	2	3	4	5	6	7	8	9	10	11		
Basic specification													Out of the Basic Specification
Electrical characteristic													Out of the DC and AC Characteristic
Mechanical characteristic													Out of the Mechanical Specification Color change : Out of Limit Appearance Specification
Optical characteristic													Out of the Appearance Standard

## 18. QUALITY GUARANTEE

### 18-1. Acceptable Quality Level

Each lot should satisfy the quality level defined as follows.

- Inspection method: MIL-STD-105E LEVEL II Normal one time sampling
- AQL

Partition	AQL	Definition
A: Major	0.4%	Functional defective as product
B: Minor	1.5%	Satisfy all functions as product but not satisfy cosmetic standard

### 18-2. Definition of 'LOT'

One lot means the delivery quantity to customer at one time.

### 18-3. Conditions of Cosmetic Inspection

- Environmental condition

The inspection should be performed at the 1m of height from the LCD module under 2 pieces of 40W white fluorescent lamps (Normal temperature 20~25°C and normal humidity 60±15%RH).

- Inspection method

The visual check should be performed vertically at more than 30cm distance from the LCD panel.

- Driving voltage

The  $V_o$  value which the most optimal contrast can be obtained near the specified  $V_o$  in the specification. (Within  $\pm 0.5V$  of the typical value at 25°C.).

## 19. INSPECTION CRITERIA

### 19-1. Module Cosmetic Criteria

No.	Item	Judgment Criterion	Partition
1	Difference in Spec.	None allowed	Major
2	Pattern peeling	No substrate pattern peeling and floating	Major
3	Soldering defects	No soldering missing No soldering bridge No cold soldering	Major Major Minor
4	Resist flaw on substrate	Invisible copper foil ( $\varnothing 0.5\text{mm}$ or more) on substrate pattern	Minor
5	Accretion of metallic Foreign matter	No soldering dust No accretion of metallic foreign matters (Not exceed $\varnothing 0.2\text{mm}$ )	Minor Minor
6	Stain	No stain to spoil cosmetic badly	Minor
7	Plate discoloring	No plate fading, rusting and discoloring	Minor
8	Solder amount	a. Soldering side of PCB Solder to form a 'Filet' all around the lead. Solder should not hide the lead form perfectly. (too much)	Minor
	1. Lead parts	b. Components side ( In case of 'Through Hole PCB' )  Solder to reach the Components side of PCB.	
	2. Flat packages	Either 'toe' (A) or 'heel' (B) of the lead to be covered by 'Filet'. Lead form to be assume over solder.	
	3. Chips	$(3/2) H \geq h \geq (1/2) H$	Minor

### 19-2. Screen Cosmetic Criteria (Non-Operating)

No.	Defect	Judgment Criterion	Partition										
1	Spots	In accordance with <i>Screen Cosmetic Criteria (Operating) No.1.</i>	Minor										
2	Lines	In accordance with <i>Screen Cosmetic Criteria (Operating) No.2.</i>	Minor										
3	Bubbles in polarizer	<table border="1"> <thead> <tr> <th>Size : d mm</th> <th>Acceptable Qty in active area</th> </tr> </thead> <tbody> <tr> <td><math>d \leq 0.3</math></td> <td>Disregard</td> </tr> <tr> <td><math>0.3 &lt; d \leq 1.0</math></td> <td>3</td> </tr> <tr> <td><math>1.0 &lt; d \leq 1.5</math></td> <td>1</td> </tr> <tr> <td><math>1.5 &lt; d</math></td> <td>0</td> </tr> </tbody> </table>	Size : d mm	Acceptable Qty in active area	$d \leq 0.3$	Disregard	$0.3 < d \leq 1.0$	3	$1.0 < d \leq 1.5$	1	$1.5 < d$	0	Minor
Size : d mm	Acceptable Qty in active area												
$d \leq 0.3$	Disregard												
$0.3 < d \leq 1.0$	3												
$1.0 < d \leq 1.5$	1												
$1.5 < d$	0												
4	Scratch	In accordance with spots and lines operating cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor										
5	Allowable density	Above defects should be separated more than 30mm each other.	Minor										
6	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-lit type should be judged with back-lit on state only.	Minor										
7	Contamination	Not to be noticeable.	Minor										

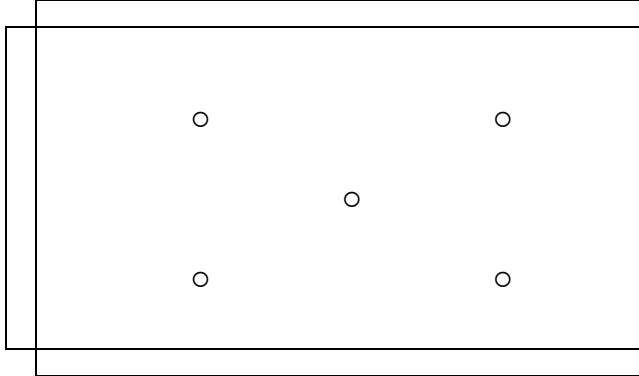
### 19-3. Screen Cosmetic Criteria (Operating)

No.	Defect	Judgment Criterion	Partition																				
1	Spots	<p>A) Clear</p> <table border="1"> <thead> <tr> <th>Size : d mm</th> <th>Acceptable Qty in active area</th> </tr> </thead> <tbody> <tr> <td><math>d \leq 0.1</math></td> <td>Disregard</td> </tr> <tr> <td><math>0.1 &lt; d \leq 0.2</math></td> <td>6</td> </tr> <tr> <td><math>0.2 &lt; d \leq 0.3</math></td> <td>2</td> </tr> <tr> <td><math>0.3 &lt; d</math></td> <td>0</td> </tr> </tbody> </table> <p>Note: Including pin holes and defective dots which must be within one pixel size.</p> <p>B) Unclear</p> <table border="1"> <thead> <tr> <th>Size : d mm</th> <th>Acceptable Qty in active area</th> </tr> </thead> <tbody> <tr> <td><math>d \leq 0.2</math></td> <td>Disregard</td> </tr> <tr> <td><math>0.2 &lt; d \leq 0.5</math></td> <td>6</td> </tr> <tr> <td><math>0.5 &lt; d \leq 0.7</math></td> <td>2</td> </tr> <tr> <td><math>0.7 &lt; d</math></td> <td>0</td> </tr> </tbody> </table>	Size : d mm	Acceptable Qty in active area	$d \leq 0.1$	Disregard	$0.1 < d \leq 0.2$	6	$0.2 < d \leq 0.3$	2	$0.3 < d$	0	Size : d mm	Acceptable Qty in active area	$d \leq 0.2$	Disregard	$0.2 < d \leq 0.5$	6	$0.5 < d \leq 0.7$	2	$0.7 < d$	0	Minor
Size : d mm	Acceptable Qty in active area																						
$d \leq 0.1$	Disregard																						
$0.1 < d \leq 0.2$	6																						
$0.2 < d \leq 0.3$	2																						
$0.3 < d$	0																						
Size : d mm	Acceptable Qty in active area																						
$d \leq 0.2$	Disregard																						
$0.2 < d \leq 0.5$	6																						
$0.5 < d \leq 0.7$	2																						
$0.7 < d$	0																						
2	Lines	<p>A) Clear</p> <p>Note : ( ) - Acceptable Qty in active area L - Length (mm) W - Width (mm) <math>\infty</math> - Disregard</p> <p>B) Unclear</p>	Minor																				

'Clear' = the shade and size are not changed by  $V_0$ .

'Unclear' = the shade and size are changed by  $V_0$ .

## 19-4. Screen Cosmetic Criteria (Operating) (Continued)

No.	Defect	Judgment Criterion	Partition
3	Rubbing line	Not to be noticeable.	
4	Allowable density	Above defects should be separated more than 10mm each other.	Minor
5	Rainbow	Not to be noticeable.	Minor
6	Dot size	To be 95% ~ 105% of the dot size (Typ.) in drawing. Partial defects of each dot (ex. pin-hole) should be treated as 'spot'. (see <i>Screen Cosmetic Criteria (Operating) No.1</i> )	Minor
7	Uneven brightness (only back-lit type module)	Uneven brightness must be $B_{MAX} / B_{MIN} \leq 2$ - $B_{MAX}$ : Max. value by measure in 5 points - $B_{MIN}$ : Min. value by measure in 5 points Divide active area into 4 vertically and horizontally. Measure 5 points shown in the following figure.  ○ : Measuring points	Minor

Note:

- (1) Size:  $d = (\text{long length} + \text{short length}) / 2$
- (2) The limit samples for each item have priority.
- (3) Complexes defects are defined item by item, but if the numbers of defects are defined in above table, the total number should not exceed 10.
- (4) In case of 'concentration', even the spots or the lines of 'disregarded' size should not allow. Following three situations should be treated as 'concentration'.
  - 7 or over defects in circle of  $\varnothing 5\text{mm}$ .
  - 10 or over defects in circle of  $\varnothing 10\text{mm}$ .
  - 20 or over defects in circle of  $\varnothing 20\text{mm}$ .

## 20. PRECAUTIONS FOR USING LCD MODULES

### 20-1. Handling Precautions

- (1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it or impact.
- (2) If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.
- (3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- (4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
- (5) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents:
  - Isopropyl alcohol
  - Ethyl alcohol
- (6) Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.
  - Water
  - Ketene
  - Aromatic solvents
- (7) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.

(8) Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the I/O cable or the backlight cable.

(9) Do not attempt to disassemble or process the LCD module.

(10) NC terminal should be open. Do not connect anything.

(11) If the logic circuit power is off, do not apply the input signals.

(12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

- Be sure to ground the body when handling the LCD modules.

- Tools required for assembling, such as soldering irons, must be properly grounded.

- To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions.

- The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

## 20-2. Storage Precautions

When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags (avoid high temperature / high humidity and low temperatures below 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

## 20-3. Others

Liquid crystals solidify under low temperature (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subject to a low temperature.

If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.

To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity etc., exercise care to avoid holding the following sections when handling the modules.

- Exposed area of the printed circuit board.

- Terminal electrode sections.

# 21. USING LCD MODULES

## 21-1. Liquid Crystal Display Modules

LCD is composed of glass and polarizer. Pay attention to the following items when handling.

(1) Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.

(2) Do not touch, push or rub the exposed polarizer with anything harder than an HB pencil lead (glass, tweezers, etc.).

(3) N-hexane is recommended for cleaning the adhesives used to attach front/rear polarizer and reflectors made of organic substances which will be damaged by chemicals such as acetone, toluene, ethanol and isopropyl alcohol.

(4) When the display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum benign. Do not scrub hard to avoid damaging the display surface.

(5) Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.

(6) Avoid contacting oil and fats.

(7) Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizer. After products are tested at low temperature they must be warmed up in a container before coming in contact with room temperature air.

(8) Do not put or attach anything on the display area to avoid leaving marks on.

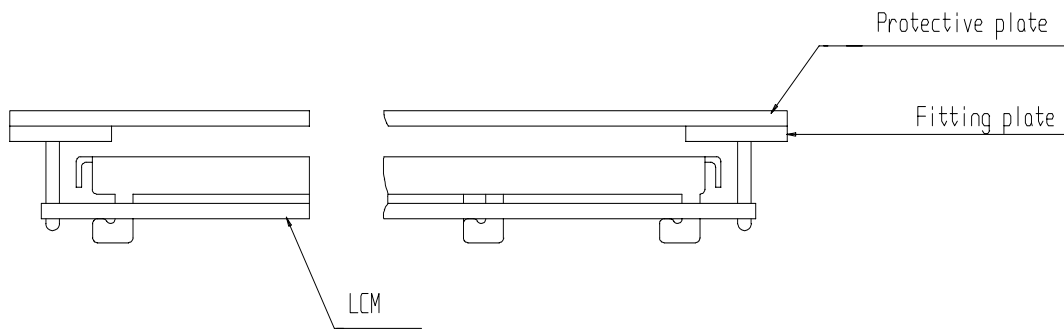
(9) Do not touch the display with bare hands. This will stain the display area and deplete insulation between terminals (some cosmetics are determinate to the polarizer).

(10) As glass is fragile. It tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring.

## 21-2. Installing LCD Modules

The hole in the printed circuit board is used to fix LCM as shown in the picture below. Attend to the following items when installing the LCM.

(1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be  $\pm 0.1\text{mm}$ .

### 21-3. Precaution for Handling LCD Modules

Since LCM has been assembled and adjusted with a high degree of precision, avoid applying excessive shocks to the module or making any alterations or modifications to it.

- (1) Do not alter, modify or change the shape of the tab on the metal frame.
- (2) Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.
- (3) Do not damage or modify the pattern writing on the printed circuit board.
- (4) Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector.
- (5) Except for soldering the interface, do not make any alterations or modifications with a soldering iron.
- (6) Do not drop, bend or twist LCM.

### 21-4. Electro-Static Discharge Control

Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

- (1) Make certain that you are grounded when handling LCM.
- (2) Before remove LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential.
- (3) When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.
- (4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced sparks coming from the commentator of the motor.
- (5) As far as possible make the electric potential of your work clothes and that of the work bench the ground potential.
- (6) To reduce the generation of static electricity is careful that the air in the work is not too dried. A relative humidity of 50%-60% is recommended.

### 21-5. Precaution for soldering to the LCM

- (1) Observe the following when soldering lead wire, connector cable and etc. to the LCM.
  - Soldering iron temperature:  $280^{\circ}\text{C} \pm 10^{\circ}\text{C}$ .
  - Soldering time: 3-4 sec.
  - Solder: eutectic solder.

If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage due to flux spatters.

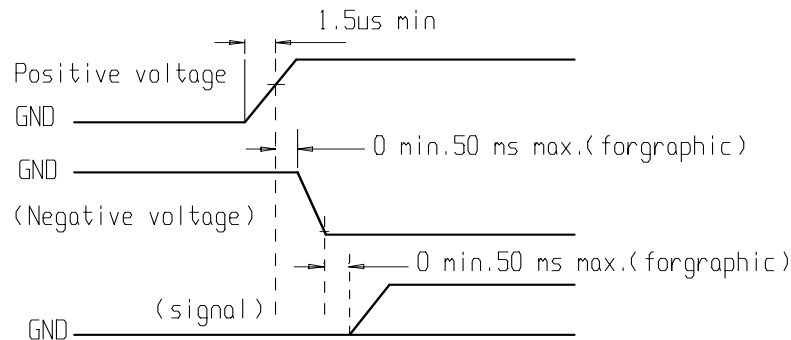
(2) When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.

(3) When remove the electroluminescent panel from the PC board, be sure the solder has completely melted, the soldered pad on the PC board could be damaged.

### 21-6. Precautions for Operation

- (1) Viewing angle varies with the change of liquid crystal driving voltage ( $V_0$ ). Adjust  $V_0$  to show the best contrast.
- (2) Driving the LCD in the voltage above the limit shortens its life.
- (3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.

- (4) If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then back on.
- (5) Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit. Therefore, it must be used under the relative condition of 40°C, 50% RH.
- (6) When turning the power on, input each signal after the positive/negative voltage becomes stable.



### 21-7. Storage

When storing LCD as spares for some years, the following precaution are necessary.

- (1) Store them in a sealed polyethylene bag. If properly sealed, there is no need for desiccant.
- (2) Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0°C and 35°C.
- (3) The polarizer surface should not come in contact with any other objects. (We advise you to store them in the container in which they were shipped.)
- (4) Environmental conditions:
  - Do not leave them for more than 168hrs. At 60°C.
  - Should not be left for more than 48hrs. At -20°C.

### 21-8. Safety

- (1) It is recommended to crush damaged or unnecessary LCD into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.
- (2) If any liquid leaks out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

### 21-9. Limited Warranty

Unless agreed between BONA and customer, BONA will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with BONA LCD acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects must be returned to BONA within 90 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of BONA limited to repair and/or replacement on the terms set forth above. BONA will not be responsible for any subsequent or consequential events.

### 21-10. Return LCM under warranty

No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are:

- Broken LCD glass.
- PCB eyelet's damaged or modified.
- PCB conductors damaged.
- Circuit modified in any way, including addition of components.
- PCB tampered with by grinding, engraving or painting varnish.
- Soldering to or modifying the bezel in any manner.

Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB eyelet's, conductors and terminals.