ISO 9001:2000 FM86067

BONA Display Specialist

BB-MG320240DLWS-02H

Product

Standard LCD Module
320 x 240 Dots graphic type
Normal temperature
STN Blue type LCD
With White LED side light

Version	Prepared / Date	Approved / Date
0	Deng lianfang 13/10-05	Zhanghong 21/10-05

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Table of Contents

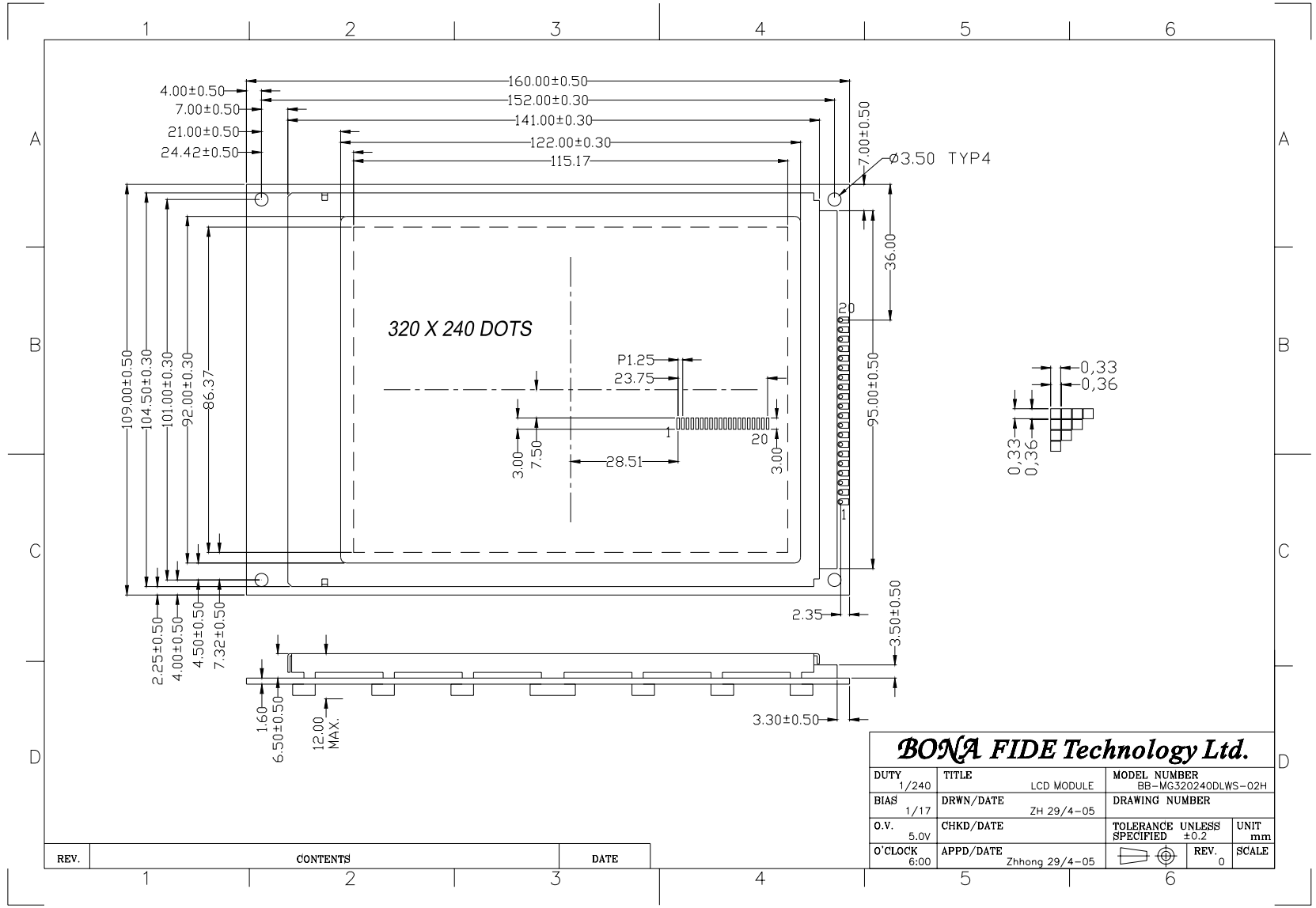
1. RECORD OF REVISION

Version	Content	Date
0	Original	13/10-05

2. PHYSICAL DATA

Item	Contents	Unit
LCD type	STN Blue, Negative Transmissive	---
LCD duty	1/240	---
LCD bias	1/17	---
Viewing direction	6	O'clock
Module size (W×H×T)	160.0 × 109.0 × 12.0MAX	mm
Viewing area (W×H)	122.0 × 92.0	mm
Number of dots	320 × 240	dots
Dot size (W×H)	0.33 × 0.33	mm
Dot pitch (W×H)	0.36 × 0.36	mm
Back light type/Color	With LED side light/ White	---

3. OUTLINE DIMENSIONS



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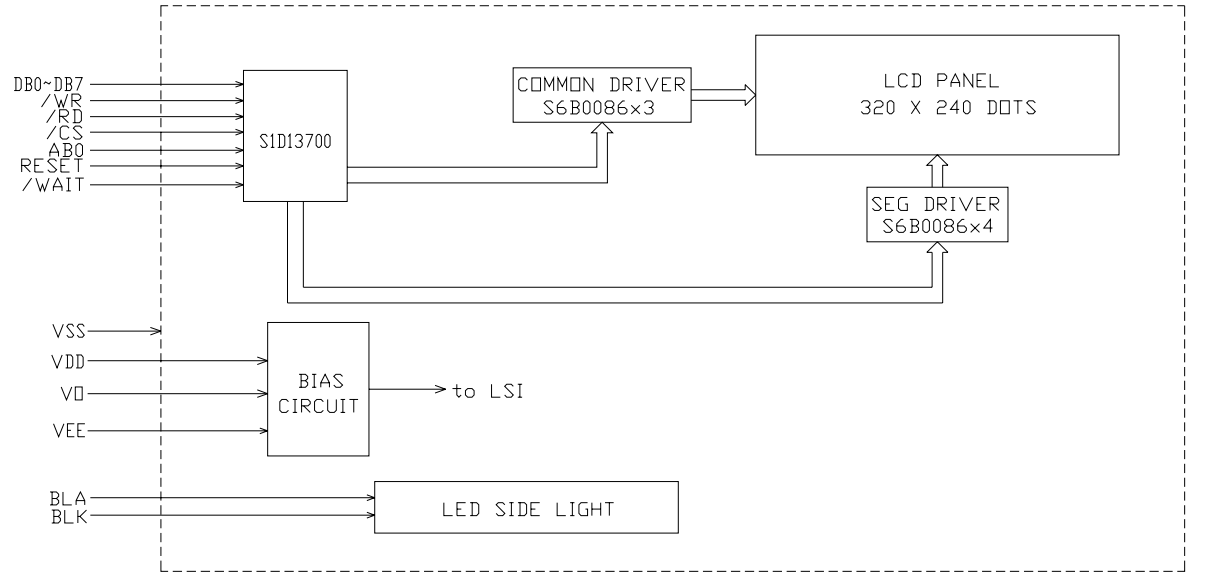
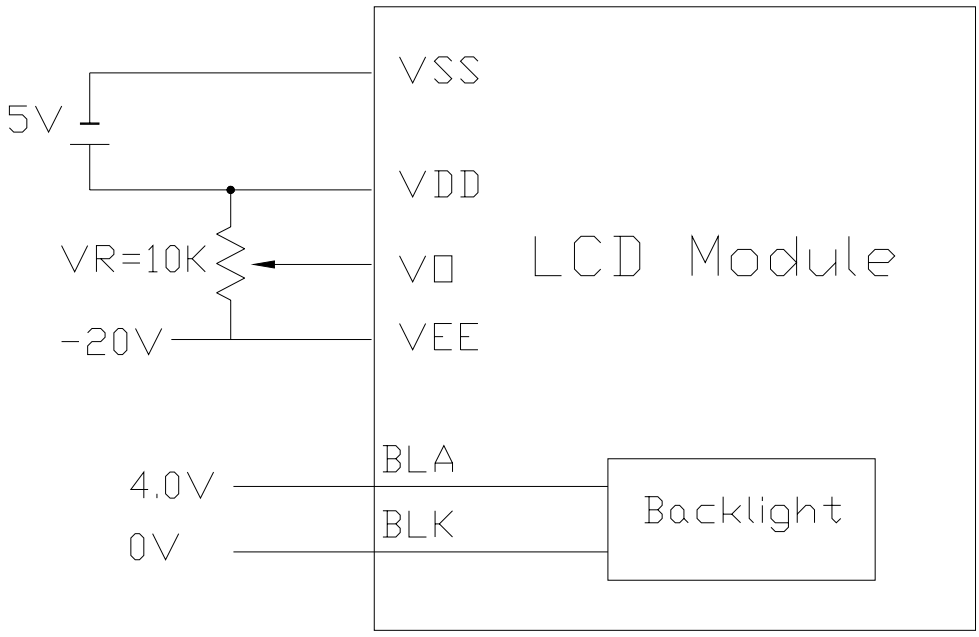
4. BLOCK DIAGRAM

The default setting of this module is 80 series, if change R23 to 10Kohm and let R24 open, this module will change to 68 series.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
VSS	VDD	VEE	V0	/WR	/RD	/CS	/WAIT	/RESET	AB0	D0	D1	D2	D3	D4	D5	D6	D7	BLA	BLK



5. POWER SUPPLY



6. ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Parameter	Symbol	Min	Max	Unit
Supply voltage for logic	V_{DD}	-0.3	7.0	V
LCD driving supply voltage	V_{EE}	0	30	V
Input voltage	VI	-0.3	V_{DD}+0.3	V
Operating temperature	T_{OP}	0	50	°C
Storage temperature	T_{ST}	-10	60	°C

7. ELECTRICAL CHARACTERISTICS (VDD = +5V±10%, VSS = 0V, Ta = 25°C)

7-1.DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage for logic	V_{DD}	---	4.5	5.0	5.5	V
Supply current for logic	I_{DD}	---	---	170	---	mA
Operating voltage for LCD	V_{EE}	25°C	22.5	23.0	23.5	V
Input voltage ' H ' level	V_{IH}	---	0.7V_{DD}	---	V_{DD}	V
Input voltage ' L ' level	V_{IL}	---	0	---	0.3V_{DD}	V

7-2.AC Characteristics

● **Reset Timing**

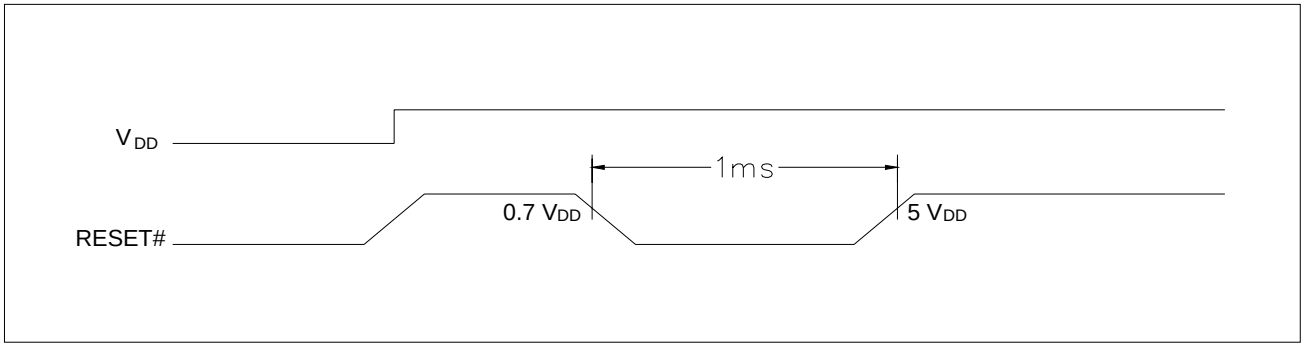


Figure 7-1 Rest Timing

The S1D13700F01 requires a reset pulse of at least 1 ms after power-on in order to reinitialize its internal state. For maximum reliability, it is not recommended to apply a DC voltage to the LCD panel while the S1D13700F01 is reset. Turn off the LCD power supplies for at least one frame period after the start of the reset pulse.

During the reset period the S1D13700F01 cannot receive commands. Commands to initialize the internal registers should be issued soon after a reset. During reset, the LCD drive signals FPDAT, FPLINE and FR are halted.

A delay of 3 ms (maximum) is required following the rising edges of both RESET# and VDD to allow for system stabilization. This delay allows the clock used by the internal oscillator circuit to become stable before use.

7-3.CPU Interface Timing

- **Generic Bus Direct/Indirect Interface with WAIT# Timing**

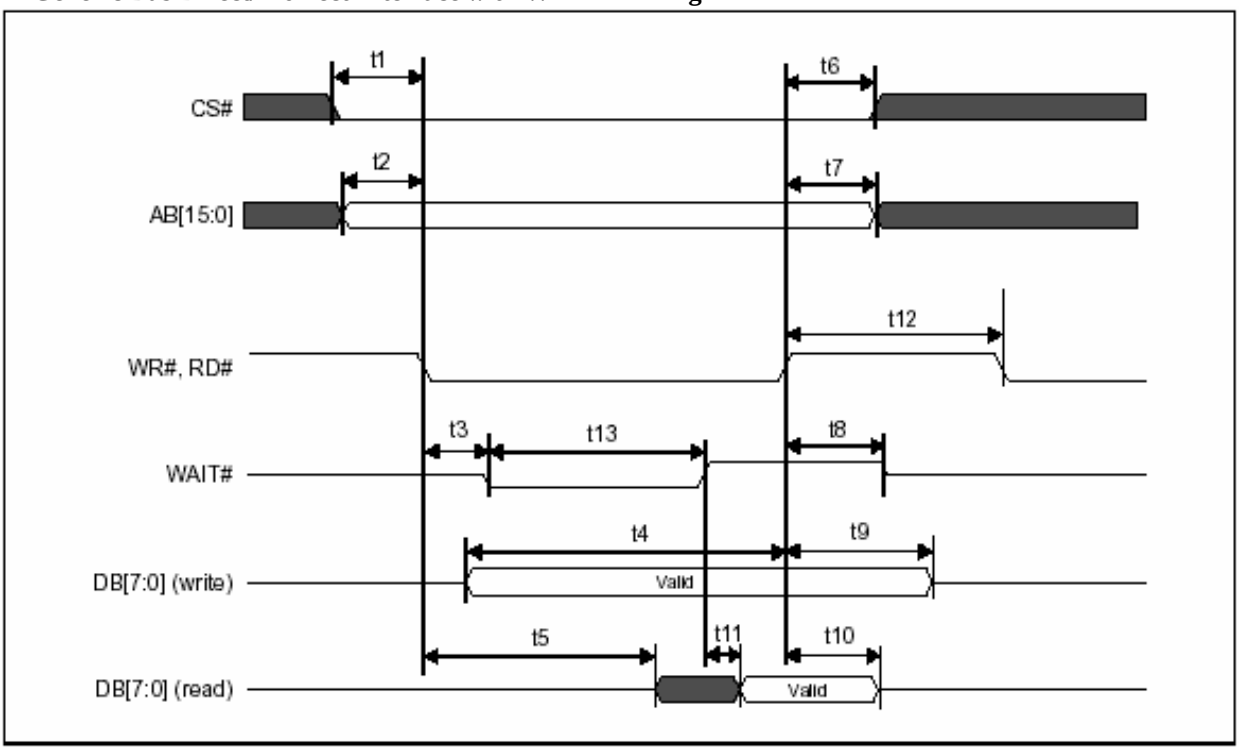


Figure 7-2 Generic Bus Direct / Indirect Interface with WAIT# Timing

Table7-1 Generic Bus Direct / Indirect Interface with WAIT# Timing

Symbol	Parameter	5.0V		Units
		Min	Max	
t1	CS# setup time	5	---	ns
t2	AB[15:0] setup time	5	---	ns
t3	WR#, RD# falling edge to WAIT# driven low	2	15	ns
t4	DB[7:0] setup time to WR# rising edge (write cycle)	Note 2	---	ns
t5	RD# falling edge to DB [7:0] driven (read cycle)	3	---	ns
t6	CS# hold time	7	---	ns
t7	AB[15:0] hold time	7	--	ns
t8	RD# WR# rising edge to WAIT# high impedance	2	10	ns
t9	DB[7:0] hold time from WR# rising edge (write cycle)	5	---	ns
t10	DB[7:0] hold time from RD# rising edge (read cycle)	3	14	ns
t11	WAIT# rising edge to valid data	---	Note 3	ns
t12	RD# WR# pulse inactive time	Note 4	---	ns
t13	Wait# pulse active time	---	Note 5	ns

Notes:
1. Ts = System clock period.
2. t4min = 2Ts + 5
3. t11max = 1Ts + 7 (for 5.0V)
4. t12min = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)
5. t13max = 4Ts + 2

● **Generic Bus Direct/Indirect Interface without WAIT# Timing**

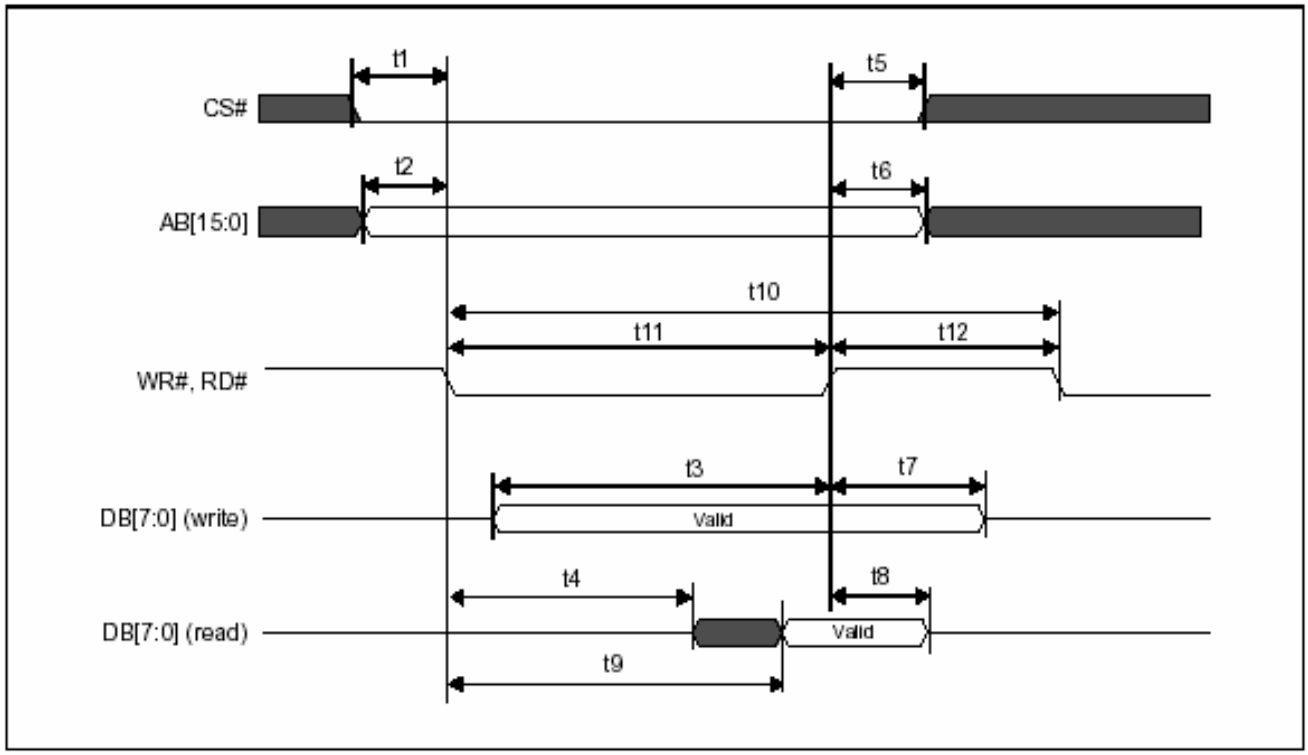


Figure 7-3 Generic Bus Direct / Indirect Interface without WAIT# Timing

Table 7-2 Generic Bus Direct / Indirect Interface without WAIT# Timing

Symbol	Parameter	5.0V		Units
		Min	Max	
t1	CS# setup time	5	---	ns
t2	AB[15:0] setup time	5	---	ns
t3	DB[7:0] setup time to WR# rising edge (write cycle)	Note 2	---	ns
t4	RD# falling edge to DB [7:0] driven (read cycle)	3	---	ns
t5	CS# hold time	7	---	ns
t6	AB[15:0] hold time	7	--	ns
t7	DB[7:0] hold time from WR# rising edge (write cycle)	5	---	ns
t8	DB[7:0] hold time from RD# rising edge (read cycle)	3	14	ns
t9	RD# falling edge to valid data (read cycle)	---	Note 3	ns
t10	RD# WR# cycle time	Note 4	---	ns
t11	RD# WR# pulse active time	5	---	Ts
t12	RD# WR# pulse inactive time	Note 5	---	ns

Notes:

1. Ts = System clock period.
2. t3min = 2Ts + 5
3. t9max = 4Ts + 20 (for 5.0V)
4. t10min = 6Ts (for a read cycle followed by a read or write cycle)
   = 7Ts + 2 (for a write cycle followed by a write cycle)
   = 10Ts + 2 (for a write cycle followed by a read cycle)
5. t12max = 1Ts (for a read cycle followed by a read or write cycle)
   = 2Ts + 2 (for a write cycle followed by a write cycle)
   = 5Ts + 2 (for a write cycle followed by a read cycle)

8. OPERATING PRINCIPLES & METHODS

8-1.Register Set

The S1D13700F01 registers are listed in the following table

Table 8-1: S1D13700F01 Register Set

Register	Pg	Register	Pg
LCD Register Description (offset = 8000h)			
System Control Registers			
REG[00h] memory configuration register	11	REG[01h] horizontal character size register	14
REG[02h] vertical character size register	15	REG[03h] character bytes per row register	15
REG[04h] total character bytes per row register	15	REG[05h] frame height register	15
REG[06h] horizontal address range register 0	15	REG[07h]horizontal address range register 1	15
REG[08h] power save mode register	16		
Display Control Registers			
REG[09h] display enable register	16	REG[0Ah] display attribute register	17
REG[0Bh] screen block 1 start address register 0	18	REG[0Ch] screen block 1 start address register 1	18
REG[0Dh] screen block 1 size register	18	REG[0Eh] screen block 2 start address register 0	18
REG[0Fh] screen block 2 start address register 1	18	REG[10h] screen block 2 size register	19
REG[11h] screen block 3 start address register 0	19	REG[12h] screen block 3 start address register 1	19
REG[13h] screen block 4 start address register 0	19	REG[14h] screen block 4 start address register 1	19
REG[15h] cursor width register	22	REG[16h] cursor height register	22
REG[17h] cursor shift direction register	23	REG[18h] overlay register	23
REG[19h] character generator RAM start address register 0	25	REG[1Ah] character generator RAM start address register 1	25
REG[1Bh] horizontal pixel scroll register	25		
Drawing Control Registers			
REG[1Ch] cursor write register 0	26	REG[1Dh] cursor write register 1	26
REG[1Eh] cursor read register 0	26	REG[1Fh] cursor read register 1	26
Gray Scale Register			
REG[20h] bit-per pixel select register	26		

8-2.Register Restrictions

All reserved bits must be set to 0 unless otherwise specified. Writing a value to a reserved bit may produce undefined results. Bits marked as n/a have no hardware affect.

8-3.Register Descriptions

- **System Control Registers**

The following registers initialize the S1D13700F01, set the window sizes, and select the LCD interface format. Incorrect configuration of these registers may cause other commands to operate incorrectly.

- **System Set**

The SYSTEM SET command is used to configure the S1D13700F01 for the display used and to exit power save mode **when indirect addressing is used.** The values from REG [00h] are passed as parameters when the SYSTEM SET command is issued.

REG[00h] Memory Configuration Register

Address = 8000h Default = 10h Read/Write

n/a	Screen Origin Compensation	Reserved	Panel Drive Select	Character Height	Reserved	Character Generator Select
7 6	5	4	3	2	1	0

Note:

When REG[00H] is written to, the S1D13700F01 automatically performs the following functions.

1. Resets the internal timing generator
2. Disables the display
3. when indirect addressing mode is selected, completes and exits power save mode

Bit 5

Screen Origin Compensation (IV)

This bit controls Screen Origin Compensation which is used for inverse display and is usually set to 1. A common method of displaying inverted characters is to Exclusive-OR the text layer with the graphics back-ground layer. However when this is done, the inverted characters at the top or left of the screen become difficult to read. This is because the character origin is at the top-left of its bitmap and there are no background pixels either above or to the left of these characters.

This bit causes the S1D13700F01 to offset the text screen against the graphics back layer by one vertical pixel. To shift the text screen horizontally, the horizontal pixel scroll function (REG[1Bh] or the HDOT SCR command for indirect addressing) can be used to shift the text screen 1 to 7 pixels to the right. If both of these functions are enabled, all characters have the appropriate surrounding back-ground pixels to ensure easy reading of the inverted characters.

When this bit = 0, screen origin compensation is done.

When this bit = 1, screen origin compensation is not done.

The following figure shows an example of screen origin compensation and the HDOT SCR command in use.

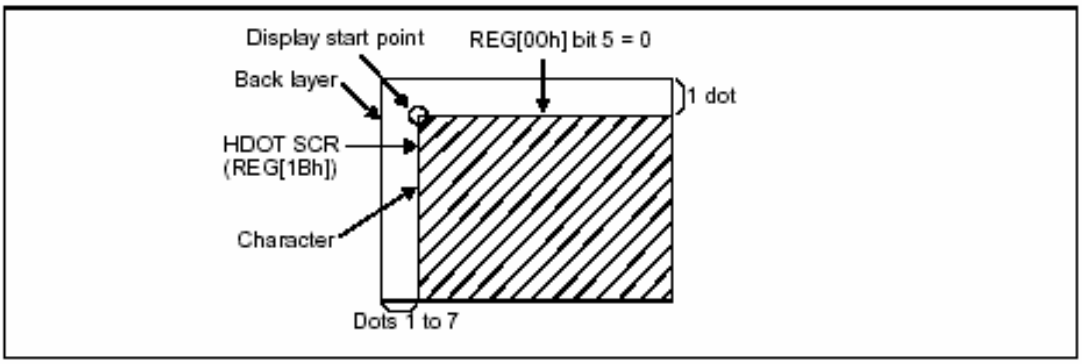


Figure 8-1 Screen Origin Compensation and HDOT SCR Adjustment

Bit 4

Reserved

The default value for this bit is 1.

Bit 3

Panel Drive Select (W/S)

This bit specifies the LCD panel drive method.

When this bit = 0, a single panel drive is selected.

The following diagrams show examples of the possible drive methods.

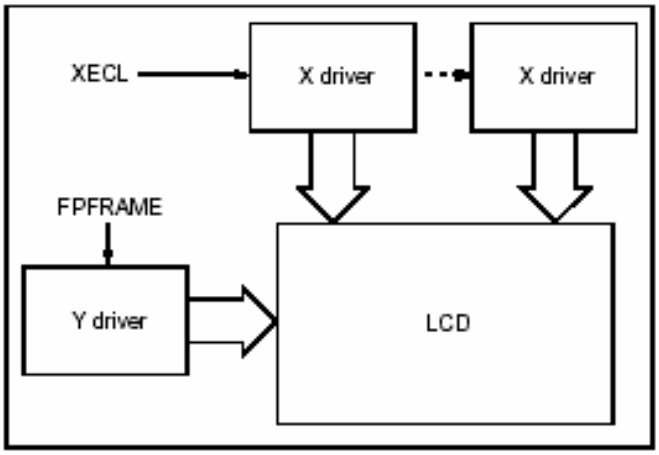


Figure 8-2 Single Drive Panel Display

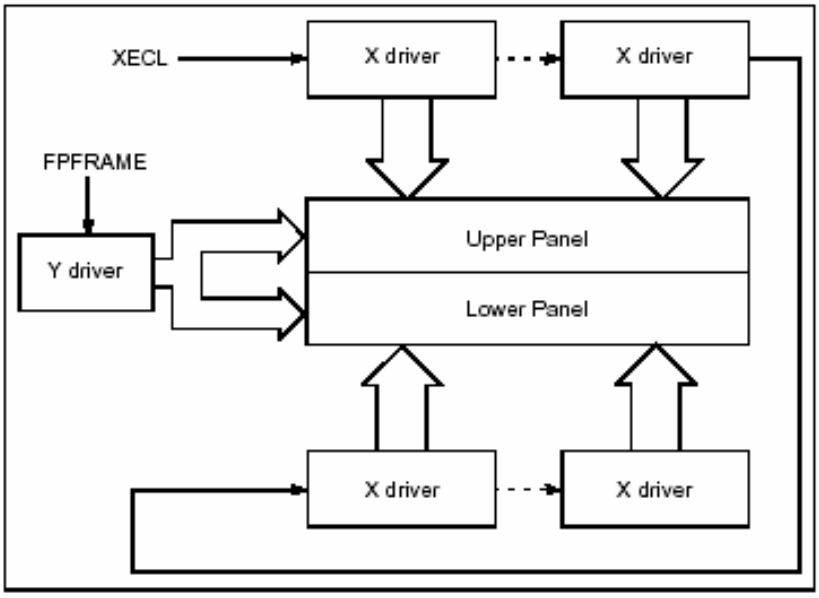


Figure 8-3 Dual Drive Panel Display

The following table summarizes the parameters that must be configured for correct operation of an LCD panel

Table 8-2 LCD parameter Summary

Parameter	Single Panel (REG[00h] bit 3 = 0)		Dual Panel (REG[00h] bit 3 = 1)	
	REG[00h] bit 5 = 1 (IV)	REG[00h] bit 5 = 0 (IV)	REG[00h] bit 5 = 1 (IV)	REG[00h] bit 5 = 0 (IV)
C/R	REG[03h] bits 7-0	REG[03h] bits 7-0	REG[03h] bits 7-0	REG[03h] bits 7-0
TC/R	REG[04h] bits 7-0	REG[04h] bits 7-0	REG[04h] bits 7-0	REG[04h] bits 7-0
L/F	REG[05h] bits 7-0	REG[05h] bits 7-0	REG[05h] bits 7-0	REG[05h] bits 7-0
SL1	00h to REG[05h] bits 7-0	00h to REG[05h] bits 7-0 (See Note)	[REG[05h] bits 7-0 + 1] ÷ 2 - 1	[REG[05h] bits 7-0 + 1] ÷ 2 - 1
SL2	00h to REG[05h] bits 7-0	00h to REG[05h] bits 7-0 (See Note)	[REG[05h] bits 7-0 + 1] ÷ 2 - 1	[REG[05h] bits 7-0 + 1] ÷ 2 - 1
SAD1	First screen block (Start Address = REG[0Bh], REG[0Ch])			
SAD2	Second screen block (Start Address = REG[0Eh], REG[0Fh])			
SAD3	Third screen block (Start Address = REG[11h], REG[12h])			
SAD4	Invalid		Fourth screen block (Start Address = REG[13h], REG[14h])	
Cursor movement range	Continuous movement over whole screen		Above-and-below configuration: continuous movement over whole screen	

Note:
Screen origin compensation shifts the character font down by one pixel row. If the bottom pixel row of the font is at the bottom of the screen block, that row disappears when REG[00h] bit 5 = 0. To compensate for the bad visual effect, SL can be increased by one.

Bit 2

Character Height (M2)

This bit selects the height of the character bitmaps. It is possible to display characters greater than 16 pixels high by creating a bitmap for each portion of each character and using graphics mode to reposition them.

When this bit = 0, the character height is 8 pixels.

When this bit = 1, the character height is 16 pixels.

Bit 1

Reserved

The default value for this bit is 0.

Bit 0

Character Generator Select (M0)

This bit determines whether characters are generated by the internal character generator ROM (CGROM) or character generator RAM (CGRAM). The CGROM contains 160, 5x7 pixel characters which are fixed at fabrication. The CGRAM can contain up to 256 user-defined characters which are mapped at the CG start

address (REG[1Ah]-REG[19h]). However, when the CGROM is used, the CGRAM can only contain up to 64, 8x8 pixel characters
When this bit = 0, the internal CGROM is selected.
When this bit = 1, the internal CGRAM is selected.
Note:
If the CGRAM is used (includes CGRAM1 and CGRAM2), only 1 bpp is supported.

REG[01h] Horizontal Character Size Register							
Address = 8001h Default = 00h							Read/Write
MOD	n/a			Horizontal Character Size bits 3-0			
7	6	5	4	3	2	1	0

Bit 7

MOD
This bit selects the AC frame drive waveform period. MOD is typically set to 1.
When this bit = 0, 16-line AC drive is selected.
When this bit = 1, two-frame AC drive is selected.
In two-frame AC drive, the MOD period is twice the frame period. In 16-line AC drive, MOD inverts every 16 lines. Although 16-line AC drive gives a more readable display, horizontal lines may appear when using high LCD drive voltages or at high viewing angles.

Bit 3-0

Horizontal character size (FX) bits [3:0]
These bits define the horizontal size, or width, of each character, in pixels.
REG[01h] BITS 3-0 = Horizontal character size in pixels-1
The S1D13700F01 handles display data in 8-bit units, therefore characters larger than 8-pixels wide must be formed from 8-pixel segments. The following diagram shows an example of a character requiring two 8-pixel segments where the remainder of the second eight bits are not displayed. This also applies to the second screen layer. In graphics mode, the normal character field is also eight pixels. If a wider character field is used, any remainder in the second eight bits is not displayed.

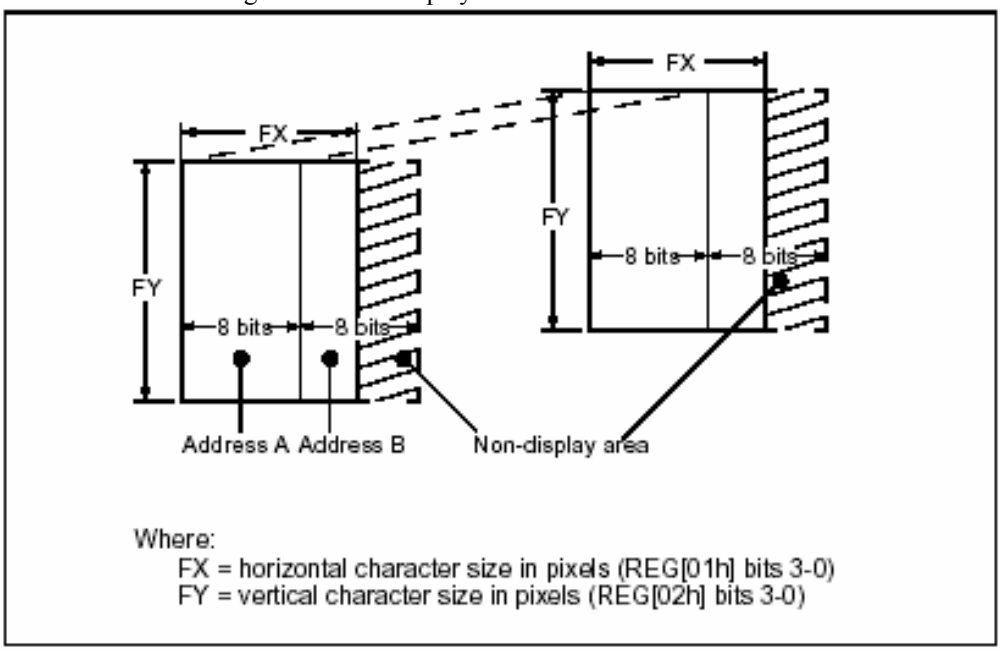


Figure 8-4 Horizontal and Vertical Character Size Example

REG[02h] Vertical Character Size Register

Address = 8002h Default = 00h Read/Write

7	6	5	4	3	2	1	0
n/a				Vertical Character Size bits 3-0			

bit 3-0 Vertical Character Size (FY) bits [3:0]

These bits define the vertical size, or height, of each character, in pixels.

REG[02h] bits 3-0 = Vertical Character Size in pixels - 1

REG[03h] Character Bytes Per Row Register

Address = 8003h Default = 00h Read/Write

7	6	5	4	3	2	1	0
Character Bytes Per Row bits 7-0							

bits 7-0 Character Bytes Per Row (C/R) bits [7:0]

These bits determine the size of each character row (or display line), in bytes, to a maximum of 239. The value of these bits is defined in terms of C/R which is calculated in Section 15.1.1, "SYSTEM SET Command and Parameters" on page 100.

REG[03h] bits 7-0 = ([C/R] x bpp) - 1

REG[04h] Total Character Bytes Per Row Register

Address = 8004h Default = 00h Read/Write

7	6	5	4	3	2	1	0
Total Character Bytes Per Row bits 7-0							

bits 7-0 Total Character Bytes Per Row (TC/R) bits [7:0]

These bits set the length of one line, including horizontal blanking, in bytes, to a maximum of 255. The value of these bits is defined in terms of TC/R which is calculated in Section 15.1.1, "SYSTEM SET Command and Parameters" on page 100. TC/R can be adjusted to hold the frame period constant and minimize jitter for any given main oscillator frequency, fosc.

REG[04h] bits 7-0 = [TC/R] + 1

Note

TC/R must be programmed such that the following formulas are valid.

$[TC/R] \geq [C/R] + 2$

$0 \leq [TC/R] \leq 255$

REG[05h] Frame Height Register

Address = 8005h Default = 00h Read/Write

7	6	5	4	3	2	1	0
Frame Height bits 7-0							

bits 7-0 Frame Height (L/F) bits [7:0]

These bits determine the frame height, in lines. The maximum frame height is 256 lines.

REG[05h] bits 7-0 = frame height in lines - 1.

Note

If the Panel Drive Select bit is set for a dual drive panel (REG[00h] bit 3 = 1), the frame height must be an even number of lines resulting in an odd number value for REG[05h] bits 7-0.

REG[06h] Horizontal Address Range Register 0

Address = 8006h Default = 00h Read/Write

7	6	5	4	3	2	1	0
Horizontal Address Range bits 7-0							

REG[07h] Horizontal Address Range Register 1

Address = 8007h Default = 00h Read/Write

7	6	5	4	3	2	1	0
Horizontal Address Range bits 15-8							

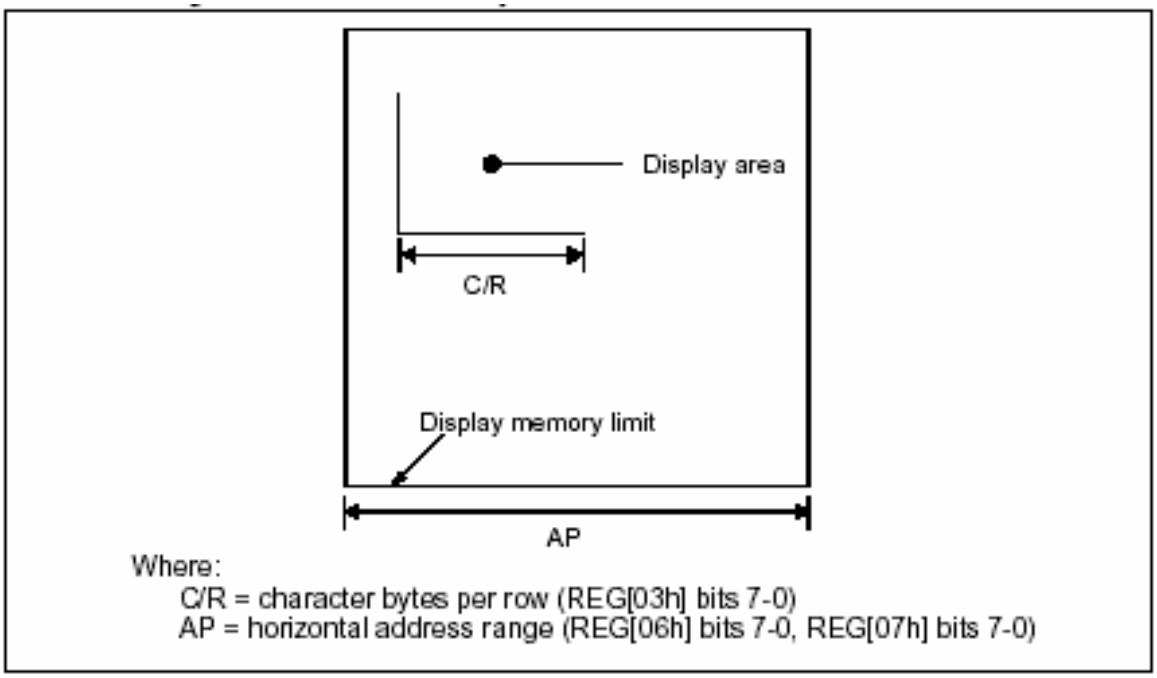


Figure 8-5 Horizontal Address Range and Character Bytes Per Row Relationship

- **Power Save**

The POWER SAVE command is used to enter power save mode on the S1D13700F01 when indirect addressing is used.

Note:

When indirect addressing is used, the SYSTEM SET command is used to exit power save mode.

REG[08h] Power Save Mode Register
Address = 8008h Default = 01h Read/Write

7	6	5	4	3	2	1	0
n/a							Power Save Mode Enable

Bit 0

Power save mode enable

This bit controls the state of the software initiated power save mode. When power save mode is disabled, the S1D13700F01 is operating normally. When power save mode is enabled, the S1D13700F01 is in a power efficient state where all internal operations, including the oscillator, are stopped.

When this bit = 0, power save mode is disabled (see note).

When this bit = 1, power save mode is enabled (default).

Note:

To fully disable power save mode when in direct mode, a dummy write to any register must be performed after setting REG[08h] bit 0 = 0.

Note:

Enabling power save mode automatically clears the display enable bit (REG[09h] bit 0). After power save mode is disabled, the display enable bit must be set (REG[09h] bit 0 = 1) in order to turn on the display again.

- **Display Control Registers**

These registers enable / disable the display, and control the cursor and layered screens.

- **Display ON / OFF**

The DISPLAY ON/FF command is used to enable / disable the display and display attributes when indirect addressing is used. The values from REG[0Ah] are passed as parameters when the DISPLAY ON/OFF command is issued.

REG[09h] Display Enable Register
Address = 8009h Default = 00h Read/Write

7	6	5	4	3	2	1	0
n/a							Display Enable

Bit 0

Display enable

This bit controls the LCD display, including the cursor and all layered screens. The display enable bit takes precedence over the individual attribute bits in the display attribute bits in the display attribute register, REG[0Ah].

REG[0Ah] Display Attribute Register

Address = 800Ah Default = 00h Read/Write

SAD3 Attribute bits 1-0		SAD2 Attribute bits 1-0		SAD1 Attribute bits 1-0		Cursor Attribute bits 1-0	
7	6	5	4	3	2	1	0

Bit 7-6

SAD3 Attribute (FP 5-4) bits [1:0]

These bits control the attributes of the third screen block (SAD3) as follows.

Table 8-3 Screen Block 3 Attribute Selection

Third Screen Block (SAD3)			
REG[0Ah] bit 7	REG[0Ah] bit 6	Attributes	
0	0	OFF (Blank)	
0	1	ON	No Flashing
1	0		Flash at f_{FR}/32 Hz (approx. 2 Hz)
1	1		Flash at f_{FR}/4 Hz (approx. 16 Hz)

Bit 5-4

SAD2 Attribute (FP 3-2) bits [1:0]

These bits control the attributes of the second screen block (SAD2). These bits also control the attributes of the fourth screen block (SAD4) when it is enabled by setting the panel drive select bit to dual panel mode (REG[00h] bit 3=1). In this mode, the attributes of the second screen block (SAD2) and the fourth screen block (SAD4) share the same settings and cannot be set independently.

Table 8-4 Screen Block 2/4 Attribute Selection

Second Screen Block (SAD2, SAD4)			
REG[0Ah] bit 5	REG[0Ah] bit 4	Attributes	
0	0	OFF (Blank)	
0	1	ON	No Flashing
1	0		Flash at f_{FR}/32 Hz (approx. 2 Hz)
1	1		Flash at f_{FR}/4 Hz (approx. 16 Hz)

Bit 3-2

SAD1 Attribute (FP 1-0) bits [1:0]

These bits control the attributes of the first screen block (SAD1) as follows.

Table 8-5 Screen Block Attribute Selection

First Screen Block (SAD1)			
REG[0Ah] bit 3	REG[0Ah] bit 2	Attributes	
0	0	OFF (Blank)	
0	1	ON	No Flashing
1	0		Flash at f_{FR}/32 Hz (approx. 2 Hz)
1	1		Flash at f_{FR}/4 Hz (approx. 16 Hz)

Bit 1-0

Cursor Attribute (FC) bits [1:0]

These bits control the cursor and set the flash rate. The cursor flashes with a 70% duty cycle (on 70% of the time and OFF 30% of the time).

Table 8-6 Cursor Flash Rate Selection

Bit 1	Bit 0	Cursor Display	
0	0	OFF (Blank)	
0	1	ON	No Flashing
1	0	ON	Flash at f_{FR}/32 Hz (approx. 2 Hz)
1	1	ON	Flash at f_{FR}/64 Hz (approx. 1 Hz)

Note:

When the cursor is disabled, a write to memory automatically enables the cursor and places the cursor at the next memory location. A read from memory does not enable the cursor; however, it still places the cursor at the next memory location.

- **SCROLL**

The scroll command is used to configure the display start addresses for the various screen blocks when indirect addressing is used. The values from REG[0Bh] through REG[14h] are passed as parameters when the Scroll command is issued.

REG[0Bh] Screen Block 1 Start Address Register 0							
Address = 800Bh Default = 00h							Read/Write
Screen Block 1 Start Address bits 7-0 (LSB)							
7	6	5	4	3	2	1	0

REG[0Ch] Screen Block 1 Start Address Register 1							
Address = 800Ch Default = 00h							Read/Write
Screen Block 1 Start Address bits 15-8 (MSB)							
7	6	5	4	3	2	1	0

Bit 15-0

Screen block 1 start address (SAD1) bits [15:0]

These bits determine the memory start address of screen block 1.

Note:

When the start address is changed, the LSB must be programmed before the MSB. The start address does not change until the MSB is written.

REG[0Dh] Screen Block 1 Size Register							
Address = 800Dh Default = 00h							Read/Write
Screen Block 1 Size bits 7-0							
7	6	5	4	3	2	1	0

Bit 7-0

Screen block 1 size (SL1) bits [7:0]

These bits determine the size of screen block 1, in lines.

REG[0Dh] bit 7-0 = screen block 1 size in number of lines -1

Note:

The relationship between the screen block start address (SADx), screen block size (SLx), and the display mode is described in Table 7-7 “Display Modes” on page 20.

REG[0Eh] Screen Block 2 Start Address Register 0							
Address = 800Eh Default = 00h							Read/Write
Screen Block 2 Start Address bits 7-0 (LSB)							
7	6	5	4	3	2	1	0

REG[0Fh] Screen Block 2 Start Address Register 1							
Address = 800Fh Default = 00h							Read/Write
Screen Block 2 Start Address bits 15-8 (MSB)							
7	6	5	4	3	2	1	0

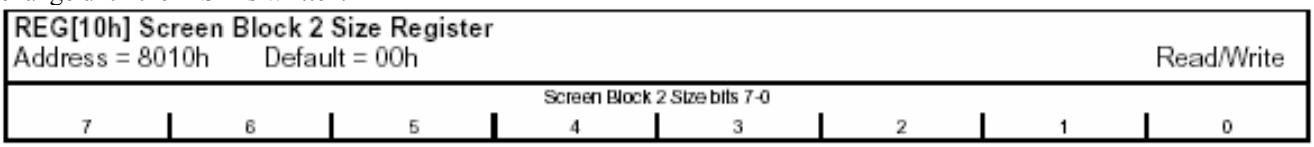
Bit 15-0

Screen block 2 start address (SAD2) bits [15:0]

These bits determine the memory start address of screen block 2.

Note:

When the start address is changed, the LSB must be programmed before the MSB. The start address does not change until the MSB is written.



Bit 7-0

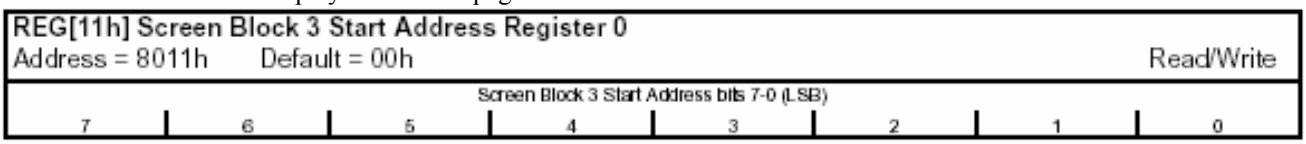
Screen block 2 size (SL2) bits [7:0]

These bits determine the size of screen block 2, in lines.

REG[10Dh] bits 7-0 = screen block 2 size in number of lines -1

Note:

The relationship between the screen block start address (SADx), screen block size (SLx), and the display mode is described in Table 7-7 “Display Modes” on page 20.



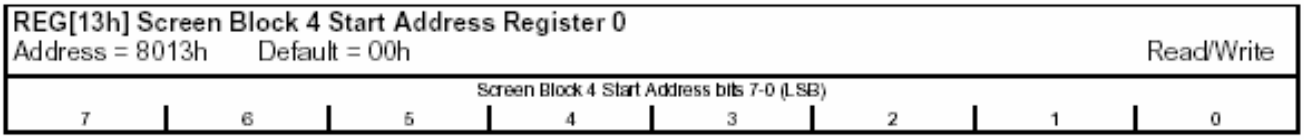
Bit 15-0

Screen block 3 start address (SAD3) bits [15:0]

These bits determine the memory start address of screen block 3.

Note:

When the start address is changed, the LSB must be programmed before the MSB. The start address does not change until the MSB is written.



Bit 15-0

Screen block 4 start address (SAD4) bits [15:0]

These bits determine the memory start address of screen block 4.

Note:

When the start address is changed, the LSB must be programmed before the MSB. The start address does not change until the MSB is written.

The following table summaries the required settings for each possible display mode.

Table 8-7 Display Modes

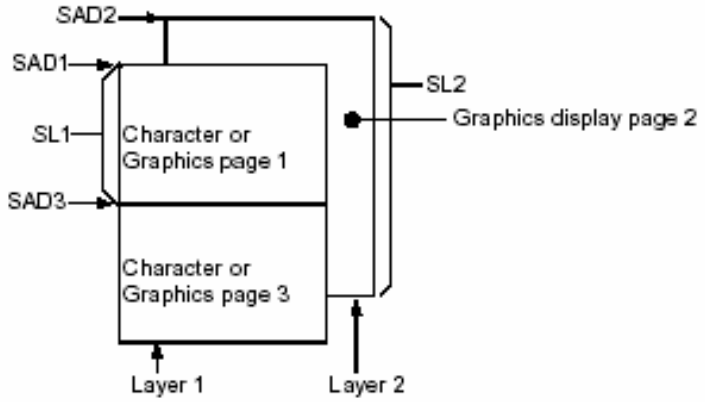
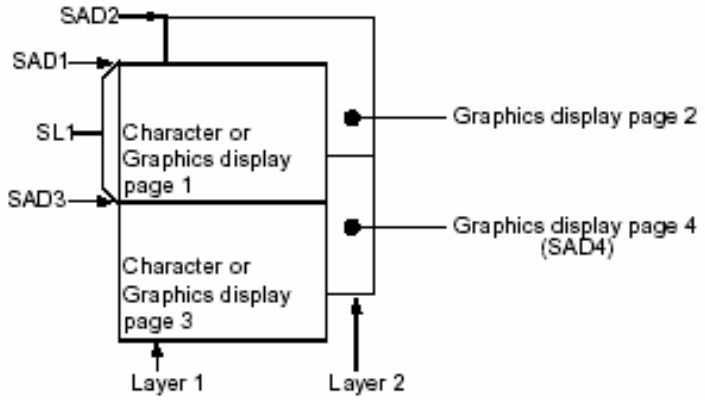
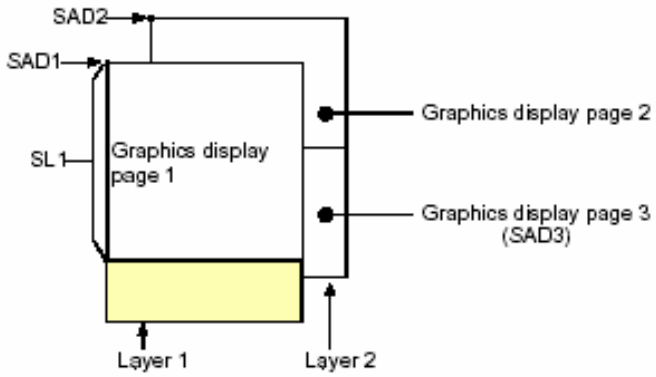
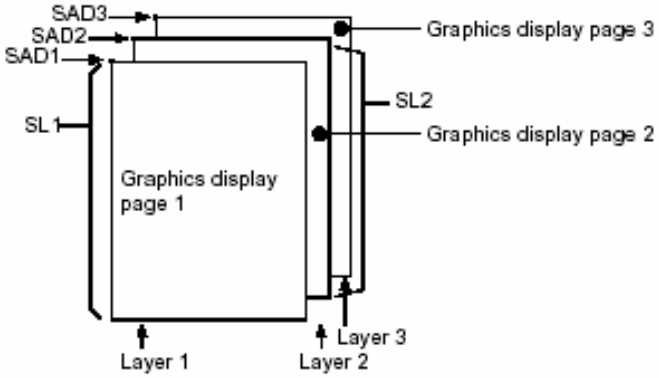
<table>
<tr><th>REG[00h] bit 3 (W/S)</th><th>Screen</th><th>First Layer</th><th>Second Layer</th></tr>
<tr><td rowspan="5">0</td><td>First Screen Block</td><td>SAD1</td><td>SAD2</td></tr>
<tr><td>Second Screen Block</td><td>SL1</td><td>SL2</td></tr>
<tr><td>Third Screen Block (partitioned screen)</td><td colspan="2">SAD3 (see note 1)
Set both SL1 and SL2 to L/F + 1 if not using a partitioned screen.</td></tr>
<tr><td colspan="3">Screen Configuration Example
 
</td></tr>
<tr><td rowspan="4">1</td><td>First Screen Block</td><td>SAD1, SL1</td><td>SAD2, SL2</td></tr>
<tr><td>Second Screen Block</td><td>SAD3 (see note 2)</td><td>SAD4 (see note 2)</td></tr>
<tr><td colspan="3">Set both SL1 and SL2 to ([L/F] ÷ 2 + 1)</td></tr>
<tr><td colspan="3">Screen Configuration Example
 
</td></tr>
</table>

Table 8-8 Display Modes (Continued)

REG[00h] bit 3 (W/S)	Screen	First Layer	Second Layer	
0	First Screen Block	SAD1, SL1	SAD2, SL2	
	Second Screen Block	—	SAD3 (see note 2)	
	Set SL1 > SL2			
	Screen Configuration Example  			
REG[00h] bit 3 (W/S)	Screen	First Layer	Second Layer	Third Layer
0	Three-Layer Configuration	SAD1, SL1 = L/F + 1	SAD2, SL2 = L/F + 1	SAD3
	Screen Configuration Example  			

Note:

1. The size of screen block 3, in lines, is automatically set to the size of the screen block with the least number of lines (either SL1 or SL2)
2. The parameters corresponding to SL3 and SL4 are fixed by REG[05h] bits 7-0 (L/F) and do not have to be set.
3. If a dual panel is selected (REG[00h] bit 3 = 1), the differences between SL1 and (L/F + 1) ÷2, are blanked.

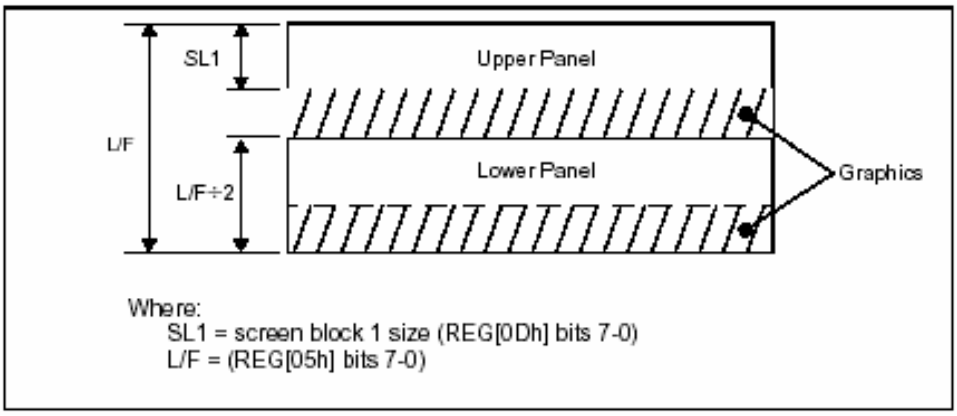


Figure 8-6 Dual Panel Display Height

- **CSRFORM**

The CSRFORM command is used to configure the S1D13700F01 cursor when indirect addressing is used. the values from REG[15h] through REG[16h] are passed as parameters when the CSRFORM command is issued.

The cursor registers are used to set the size, shape, and position of the cursor. Although the cursor is normally only used for text displays, it may be used for graphics displays when displaying special characters.

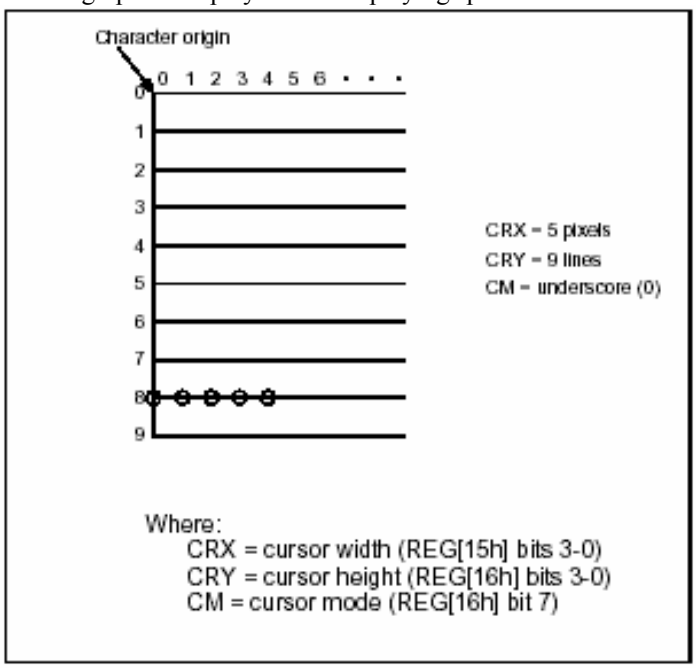


Figure 8-7 Cursor Size and Position

REG[15h] Cursor Width Register
Address = 8015h Default = 00h Read/Write

n/a				Cursor Width bits 3-0			
7	6	5	4	3	2	1	0

Bit 3-0

Cursor width (CRX) bits [3:0]

These bits specify the width (or horizontal size) of the cursor, in pixels from the character origin (see Figure 7-7 “Cursor size and position,”).

Note:

The cursor width must be less than or equal to the horizontal character size.

(REG[16h] bits 3-0 < = REG[01h] bits 3-0)

REG[16h] Cursor Height Register
Address = 8016h Default = 00h Read/Write

Cursor Mode	n/a			Cursor Height bits 3-0			
7	6	5	4	3	2	1	0

Bit 7

Cursor mode (CM)

This bit determines the cursor mode. When graphics mode is selected, this bit must be set to 1.

When this bit = 0, an underscore cursor (_) is selected.

When this bit = 1, a block cursor (■) is selected.

Bit 3-0

Cursor height (CRY) bits [3:0]

For an underscore cursor (REG[16h] bit 7 = 0), these bits set the location of the cursor, in lines from the character origin (see Figure 7-7 “Cursor size and position,”)

For a block cursor (REG[16h [bit 7 = 1], these bits set the height (or vertical size) of the cursor, in lines from the character origin (see Figure 7-7 “Cursor size and position,”).

REG[16h] bits 3-0 = cursor height in lines - 1

Note:

The vertical cursor size must be less than or equal to the vertical character size.

(REG[16h] bits 3-0 < = REG[02h] bits 3-0)

● **CSRDIR**

The CSRDIR command controls cursor movement when indirect addressing is used. The values from REG[17h] are passed as part of the command when the command when the CSRDIIR command is issued.

REG[17h] Cursor Shift Direction Register Address = 8017h Default = 00h							Read/Write
n/a						Cursor Shift Direction bits 1-0	
7	6	5	4	3	2	1	0

Bit 1-0

Cursor shift direction bits [1:0]

These bits set the direction of automatic cursor increment when the cursor is automatically moved after a memory access (read or write). The cursor can move left/right by one character or up/down by the number of bytes specified by the horizontal address range (or address pitch), REG[06h] – REG[07h]. When reading from and writing to display memory this automatic cursor increment controls the display memory address increment on each read or write.

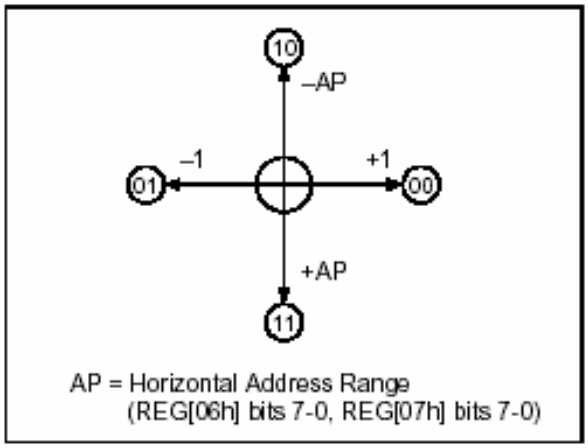


Figure 8-8 Cursor Direction

Table 8-9 Cursor Shift Direction

Direct Mode		Indirect Mode Command	Shift Direction
Bit 1	Bit 0		
0	0	4C	Right
0	1	4D	Left
1	0	4E	Up
1	1	4F	Down

Note:

The cursor moves in address units even if horizontal character size is equal to 9 (REG[01h] bits 3-0 = 9), therefore the cursor address increment must be preset for movement in character units.

● **OVLAY**

The OVLAY command selects layered screen composition and screen text/graphics mode when indirect addressing is used. the values from REG[18h] are passed as parameters when the OVLAY command is issued.

REG[18h] Overlay Register Address = 8018h Default = 00h								Read/Write
n/a			3 Layer Overlay Select	Screen Block 3 Display Mode	Screen Block 1 Display Mode	Layer Composition Method bits 1-0		
7	6	5	4	3	2	1	0	

Bit 4

3 Layer overlay select (OV)

This bit determines how many layers are used when graphics mode is enabled. For mixed test and graphics, this bit must be set to 0.

When this bit = 0, two layers are used.

When this bit = 1, three layers are used.

Bit 3

Screen block 3 display mode (DM1)
This bit determines the display mode for screen block3.
When this bit = 0, screen block 3 is configured for text mode.
When this bit = 1, screen block 3 is configured for graphics mode.

Note:

Screen blocks 2 and 4 can display graphics only.

Bit 2

Screen block 1 display mode (DM0)
This bit determines the display mode for screen block 1.
When this bit = 0, screen block 1 is configured for text mode.
When this bit = 1, screen block 1 is configured for graphics mode.

Note:

Screen blocks 2 and 4 can display graphics only.

Bit 1-0

Layer composition method (MX) bits [1:0]
These bits select the layered screen composition method, which can be OR, AND, or exclusive-OR. Since the screen composition is organized in layers and not by screen blocks, when using a layer divided into two screen blocks, different composition methods cannot be specified for the individual screen blocks.

Table 8-10 Composition Method Selection

REG[18h] bit 1	REG[18h] bit 0	Function	Composition Method	Applications
0	0	L1 ∪ L2 ∪ L3	OR	Underlining, rules, mixed text and graphics
0	1	(L1 ⊕ L2) ∪ L3	Exclusive-OR	Inverted characters, flashing regions, underlining
1	0	(L1 ∩ L2) ∪ L3	AND	Simple animation, three-dimensional appearance
1	1	—	—	Reserved

Note:

L1: First layer (text or graphics). If test is selected, layer L3 cannot be used.
L2: Second layer (graphics only)
L3: Third layer (graphics only)

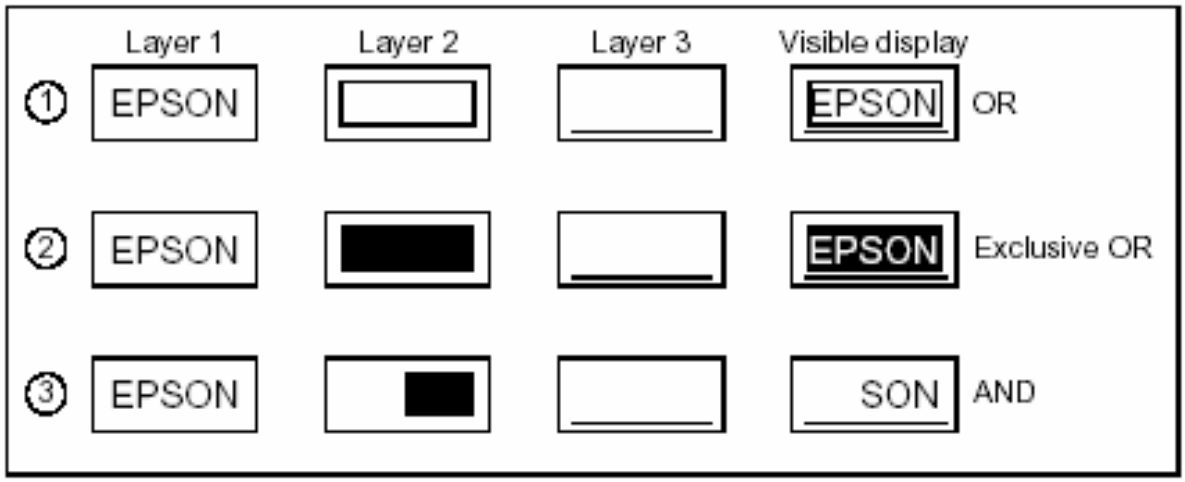


Figure 8-9 Combined Layer Display Examples

Note:

L1: Not flashing
L2: Flashing at 1 Hz
L3: Flashing at 2 Hz

● **CGRAM ADR**

The CGRAM ADR command sets the start address of the character generator RAM (CGRAM) when indirect addressing is used. The values from REG[19h] through REG[1Ah] are passed as parameters when the CGRAM ADR command is issued.

REG[19h] Character Generator RAM Start Address Register 0							
Address = 8019h Default = 00h							Read/Write
CGRAM Start Address bits 7-0 (LSB)							
7	6	5	4	3	2	1	0

REG[1Ah] Character Generator RAM Start Address Register 1							
Address = 801Ah Default = 00h							Read/Write
CGRAM Start Address bits 15-8 (MSB)							
7	6	5	4	3	2	1	0

Bit 15-0

Character generator RAM start address bits [15:0]

These bits determine the memory start address of the character generation RAM (CGRAM). The exact memory location of the start of each character stored in CGRAM can be calculated by multiplying the character code index by the character height and adding the total to the CGRAM start address.

● **HDOT SCR**

The HDOT SCR command sets the horizontal scroll position when indirect addressing is used. The values from REG[1Bh] are passed as parameters when the HDOT SCR command is issued.

Normal scrolling on text screens allows scrolling of entire characters only. The HDOT SCR command provides horizontal pixel scrolling for text screens. HDOT SCR cannot be used on individual layers.

Note:

HDOT SCR must be set to zero for all display modes except 1 bpp (REG[20h] bit-per-pixel select register bits 1-0 = 0).

REG[1Bh] Horizontal Pixel Scroll Register							
Address = 801Bh Default = 00h							Read/Write
n/a					Horizontal Pixel Scroll bits 2-0		
7	6	5	4	3	2	1	0

Bit 2-0

Horizontal pixel scroll bits [2:0]

These bits specify the number of horizontal pixels to scroll display. The character bytes per row (C/R), REG[03h] bits 7-0, must be set to one more than actual number of horizontal characters before using horizontal pixel scroll. Smooth scrolling can be simulated by repeatedly charging the value of REG[1Bh] bits 2-0. see section 12.5,"Scrolling" on page 89 for more information on scrolling the display.

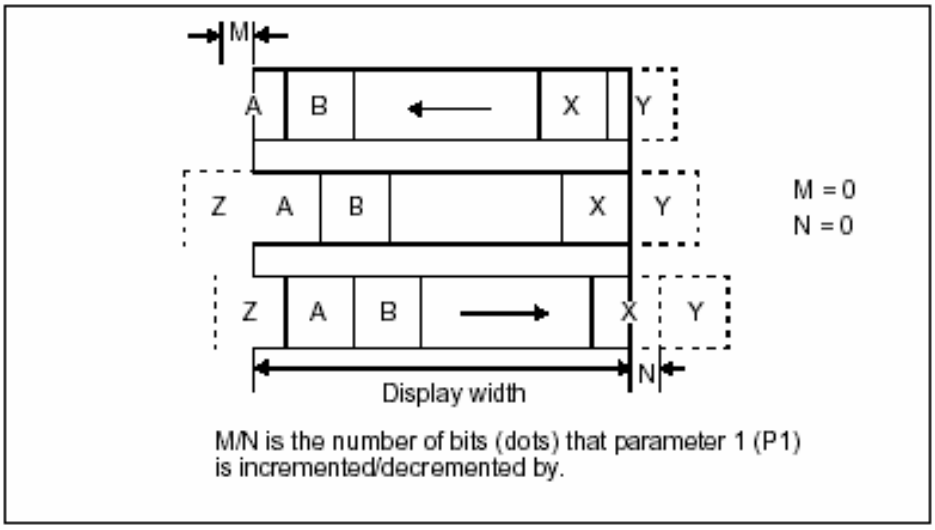
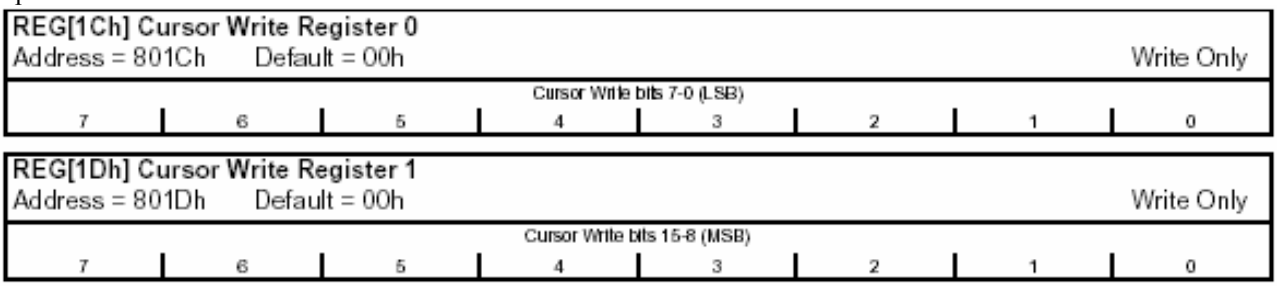


Figure 8-10 Horizontal Scrolling

8-3.1 Drawing Control Registers

- **CSRW**

The CSRW command sets the cursor address when indirect addressing is used. The values from REG[1Dh] are passed as parameters when the CSRW command is issued.



Bit 15-0

Cursor Write (CSRW) bits [15:0]

These bits set the display memory address to the data at the cursor position as shown in Figure 7-20 “Cursor Movement,” on page73.

Note

The microprocessor cannot directly access the display memory in indirect addressing mode.

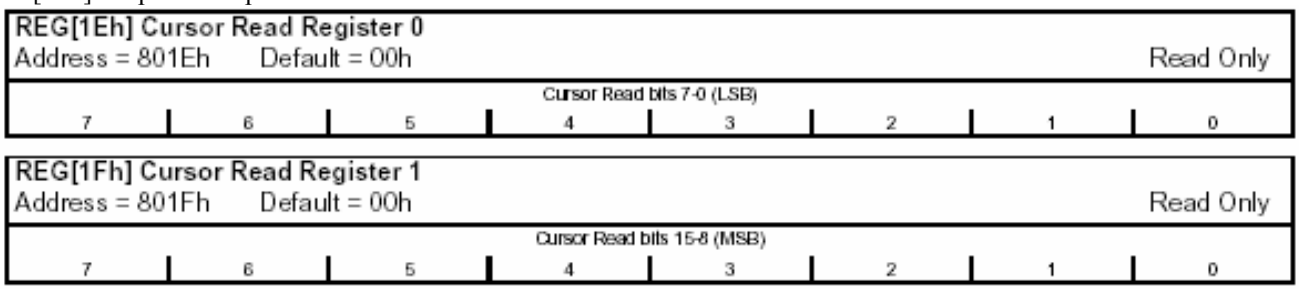
For Indirect Addressing Mode:

The MREAD and MWRITE commands use the address in this register when in indirect mode. The cursor address register can only be modified by the CSRW command and by the automatic increment after an MREAD or MWRITE command. It is not affected by display scrolling.

If a new address is not set, display memory accesses are from the last set address or the address after previous automatic increments.

- **CSRR**

The CSRR command reads the cursor address when indirect addressing is used. the values from REG[1Eh] through REG[1Fh] are passed as parameters when the CSRR command is issued.



bits 15-0 Cursor Read (CSRR) bits [15:0]

These bits are only used in Indirect Addressing mode.

These bits indicate the memory address where the cursor is currently located. After issuing the command, the data read address is read twice. Once for the low byte and then again for the high byte of the register.

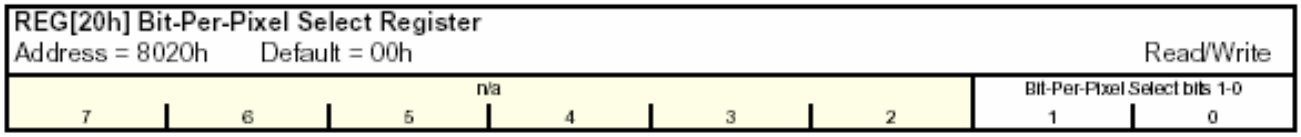
8-3.2 Gray Scale Register

- **GRAYSCALE**

The GRAYSCALE command selects the gray scale depth, in bits-per-pixel (bpp), when indirect addressing is used. the values from REG[20h] are passed as parameters when the GRAYSCALE command is issued.

Note

When a graphics screen and a graphics screen with Gray scale enabled are overlaid, both layers must be configured for the same color depth. For example, if the first layer is 2 bpp, the second layer must also be set for 2 bpp.



Bit 1-0

Bit-Per-Pixel Select bits [1:0]

These bits select the bit-per-pixel mode as follows. If the CGRAM is used (includes CGRAM 1 and CGRAM2), only 1 bpp is supported

Table 8-11 Bit-Per Pixel Selection

REG[20h] bits 1-0	Bits-Per-Pixel
00	1
01	2
10	4
11	Reserved

Note

The horizontal character size (REG[01h] bits 3-0) must be set to 7h and the Horizontal pixel scroll bits (REG[1Bh] bits 2-02) must be set to 0.

8-4 Indirect Addressing

Table 8-12 Indirect Addressing Command Set

Class	Register Address	Command	Register Description	Control Byte Value	No. of Bytes
System Control	8000h - 8007h	SYSTEM SET	Initializes device and display	40h	8
	8008h	POWER SAVE	Enters standby mode	53h	0
Display Control	8009h - 800A	DISP ON/OFF	Enables/disables display and display attributes	58h 59h	1
	800Bh - 8014h	SCROLL	Sets screen block start addresses and sizes	44h	10
	8015h - 8016h	CSRFORM	Sets cursor type	5Dh	2
	8017h	CSRDIR	Sets direction of cursor movement	4Ch - 4Fh	0
	8018h	OVLAY	Sets display overlay format	5Bh	1
	8019h - 801Ah	CGRAM ADR	Sets start address of character generator RAM	5Ch	2
	801Bh	HDOT SCR	Sets horizontal scroll position	5A	1
Drawing Control	801Ch - 801Dh	CSRW	Sets cursor address	46h	2
	801Eh - 801Fh	CSRR	Reads cursor address	47h	2
	8020h	GRAYSCALE	Sets the Grayscale depth (bpp)	60h	1
Memory Control		MEMWRITE	Writes to memory	42h	n/a
		MEMREAD	Reads from memory	43h	

Table 8-13 Generic Indirect Addressing Command / Write /Read

A0	$\overline{WR}$	$\overline{RD}$	
1	0	1	Command [C]
1	1	0	Parameter Read [P#]
0	0	1	Parameter Write [P#]

● **System set**

See section, “SYSTEM SET “on page11 for further information.

Note

If the S1D13700F01 is in power save mode (at power up or after a POWER SAVE command), the SYSTEM SET command will exit power save mode. After writing the SYSTEM SET command and its 8 parameters, the S1D13700F01 will be in normal operation.

Table 8-14 SYSTEM SET Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0	Indirect
0	1	0	0	0	0	0	0	C
0	0	IV[1]	0	W/S[2]	M2[3]	0	M0[4]	P1
MOD[5]	0	0	0	REG[01h] bits 3-0				P2
0	0	0	0	REG[02h] bits 3-0				P3
REG[03h] bits 7-0								P4
REG[04h] bits 7-0								P5
REG[05h] bits 7-0								P6
REG[06h] bits 7-0								P7
REG[07h] bits 7-0								P8

Note

1. IV is the screen origin compensation bit, REG[00h] bit 5.
2. W/S is the panel drive select bit, REG[00h] bit 3.
3. M2 is the character height bit, REG[00h] bit 2.
4. M0 is the character generator select bit, REG[00h] bit 0.
5. MOD is defined by REG[01h] bit 7.

● **Power Save**

See section. “POWER SAVE” on page 16 for further information.

Table 8-15 POWER SAVE Command

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0	Indirect
0	1	0	1	0	0	1	1	C

● **DISP ON/OFF**

The following parameters are used for the DISP ON command. For further details, see section, “DISP ON/OFF” on page 16.

Table 8-16 IDSP ON Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0	Indirect
0	1	0	1	1	0	0	1	C
REG[0Ah] bits 7-0								P1

The following parameters are used for the DISP OFF command. For further details, see section, “DISP ON/OFF” on page 16.

Table 8-17 IDSP OFF Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0	Indirect
0	1	0	1	1	0	0	0	C
REG[0Ah] bits 7-0								P1

- **SCROLL**

See "SCROLL" on page 18 for further information.

Table 8-18 SCROLL Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0		Indirect
0	1	0	0	0	1	0	0		C
A7	A6	A5	A4	A3	A2	A1	A0	REG[0Bh] bits 7-0	P1
A15	A14	A13	A12	A11	A10	A9	A8	REG[0Ch] bits 7-0	P2
L7	L6	L5	L4	L3	L2	L1	L0	REG[0Dh] bits 7-0	P3
A7	A6	A5	A4	A3	A2	A1	A0	REG[0Eh] bits 7-0	P4
A15	A14	A13	A12	A11	A10	A9	A8	REG[0Fh] bits 7-0	P5
L7	L6	L5	L4	L3	L2	L1	L0	REG[10h] bits 7-0	P6
A7	A6	A5	A4	A3	A2	A1	A0	REG[11h] bits 7-0	P7
A15	A14	A13	A12	A11	A10	A9	A8	REG[12h] bits 7-0	P8
A7	A6	A5	A4	A3	A2	A1	A0	REG[13h] bits 7-0	P9
A15	A14	A13	A12	A11	A10	A9	A8	REG[14h] bits 7-0	P10

- **CSRFORM**

See "SCRFORM" on page 22 for further information.

Table 8-19 CSRFORM Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0	Indirect
0	1	0	1	1	1	0	1	C
0	0	0	0	REG[15h] bits 3-0 X3	X2	X1	X0	P1
CM[1]	0	0	0	REG[16h] bits 3-0 Y3	Y2	Y1	Y0	P2

Note

CM is the Cursor mode bit, REG[16h] bit 7.

- **CSRDIR**

See "CSRDIR" on page 23 for further information.

Table 8-20 CSRDIR Command

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0	Indirect
0	1	0	0	1	1	REG[17h] bits 1-0 CD1	CD0	C

● **OVLAY**

See “OVLAY” on page 23 for further information.

Table 8-21 OVLAY Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0	Indirect
0	1	0	1	1	0	1	1	C
0	0	0	OV[1]	DM2[2]	DM1[2]	MX1[3]	MX0[3]	P1

Note

[1] OV is the 3 Layer Overlay Select bit, REG[18h] bit 4.

[2] DM2 and DM1 are the Screen Block 3/1 Display Mode bits, REG[18h] bits 3-2.

[3] MX1 and MX0 are the Layer Composition Method bits, REG[18h] bits 1-0.

● **CGRAM ADR**

See “CGRAM ADR” on page 25 for further information.

Table 8-22 CGRAM ADR Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0		Indirect
0	1	0	1	1	1	0	0		C
A7	A6	A5	A4	A3	A2	A1	A0	(SAGL)	P1
A15	A14	A13	A12	A11	A10	A9	A8	(SAGH)	P2

● **HDOT SCR**

See “HDOT DCR” on page 25 for further information.

Table 8-23 HDOT SCR Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0	Indirect
0	1	0	1	1	0	1	0	C
0	0	0	0	0	D2	D1	D0	P1

● **CSRW**

See “CSRW” on page 26 for further information.

Table 8-24 CSRW Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0		Indirect
0	1	0	0	0	1	1	0		C
A7	A6	A5	A4	A3	A2	A1	A0	(CSRL)	P1
A15	A14	A13	A12	A11	A10	A9	A8	(CSRH)	P2

● **CSRR**

See “CSRR” on page 26 for further information.

Table 8-25 CSRR Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0		Indirect
0	1	0	0	0	1	1	1		C
A7	A6	A5	A4	A3	A2	A1	A0	(CSRL)	P1
A15	A14	A13	A12	A11	A10	A9	A8	(CSRH)	P2

● **GRAYSCALE**
See “GRAYSCALE” on page 26 for further information.

Table 8-26 GRAYSCALE Command and Parameters

MSB							LSB	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Indirect
0	1	1	0	0	0	0	0	C
0	0	0	0	0	0	BPP1	BPP0	P1

● **Memory Control**
See “Drawing control registers” on page 26 for further information.

8-5 Display Control Functions

The origin of each character bitmap is the top left corner as shown in Figure 12-1. adjacent bits in each byte are horizontally adjacent in the corresponding character image.
Although the size of the bitmap is fixed by the character generator, the actual displayed size of the character field can be varied in both dimensions.

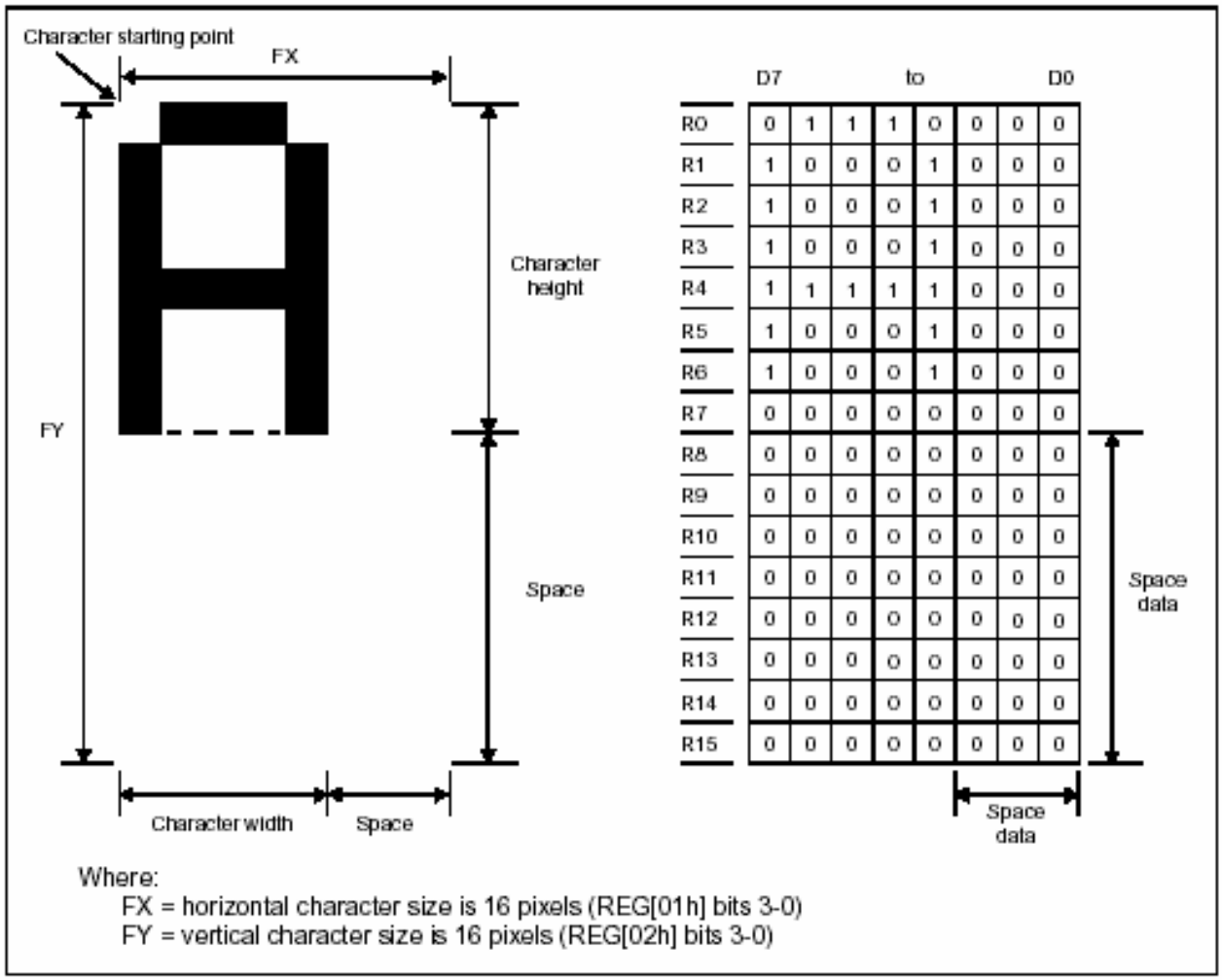


Figure 8-11 Example of Character Display from Generator Bitmap (when [FX] ≤8)

If the area outside the character bitmap contains only zeros, the display character size can be increased by increasing the horizontal character size (REG[01h] bits 3-0) and the vertical character size (REG [01h] bits 3-0). The zeros ensure that the extra space between displayed character is blank.

The displayed character width can be set to any value up to 16 even if each horizontal row of the bitmap is two bytes wide.

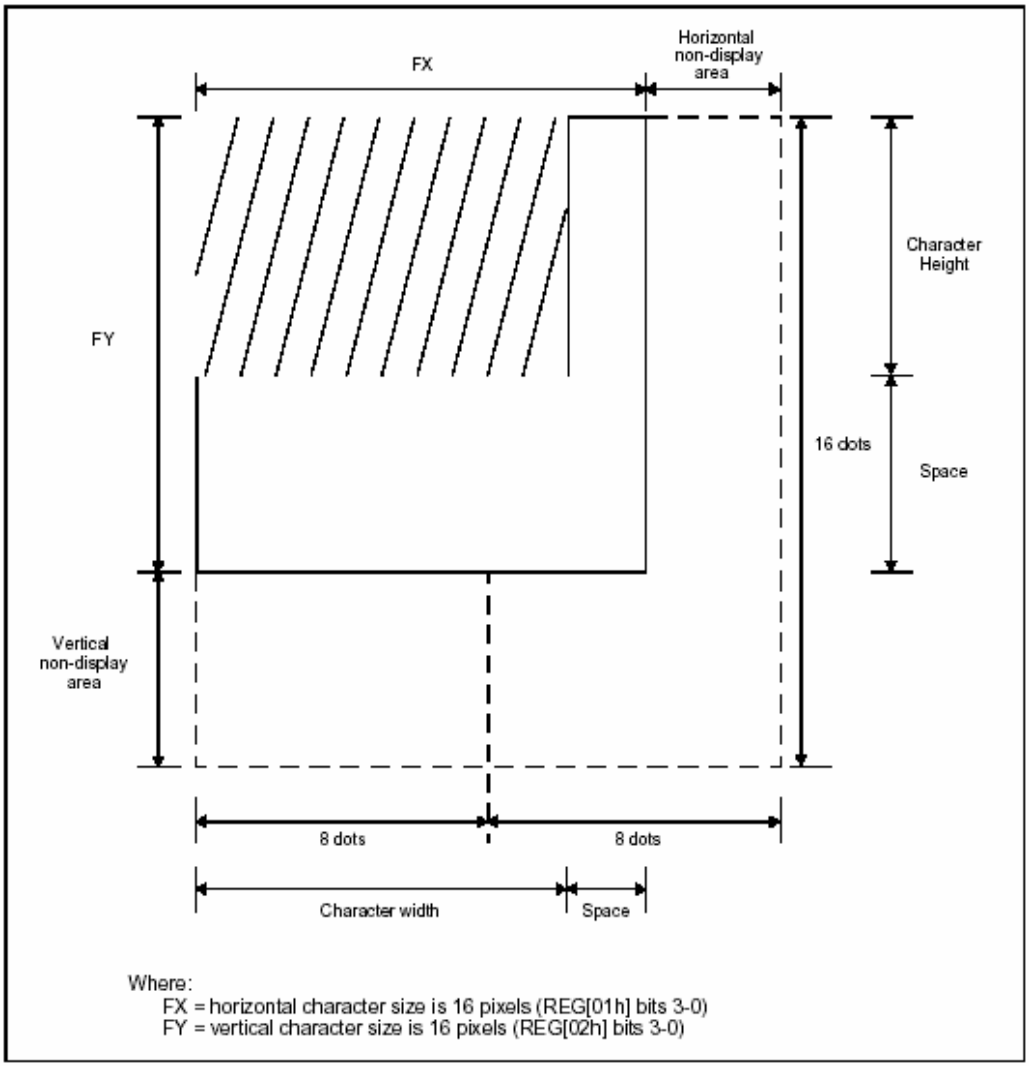


Figure 8-12 Character Width Greater than One Byte Wide ([FX] = 9)

The S1D13700F01 does not automatically insert spaces between characters. If the displayed character size is 8 pixels or less and the space between character origins is nine pixels or more, the bitmap must use two bytes per row, even though the character image requires only one.

8-6 Screen Configuration

● **Screen Configuration**

The S1D13700F01 can be configured for a single text screen, overlapping text screens, of overlapping graphics screens; Graphics screens use eight times as much display memory as a text screen in 1 bpp. Figure 12-3 shows the relationship between the virtual screens and the physical screen.

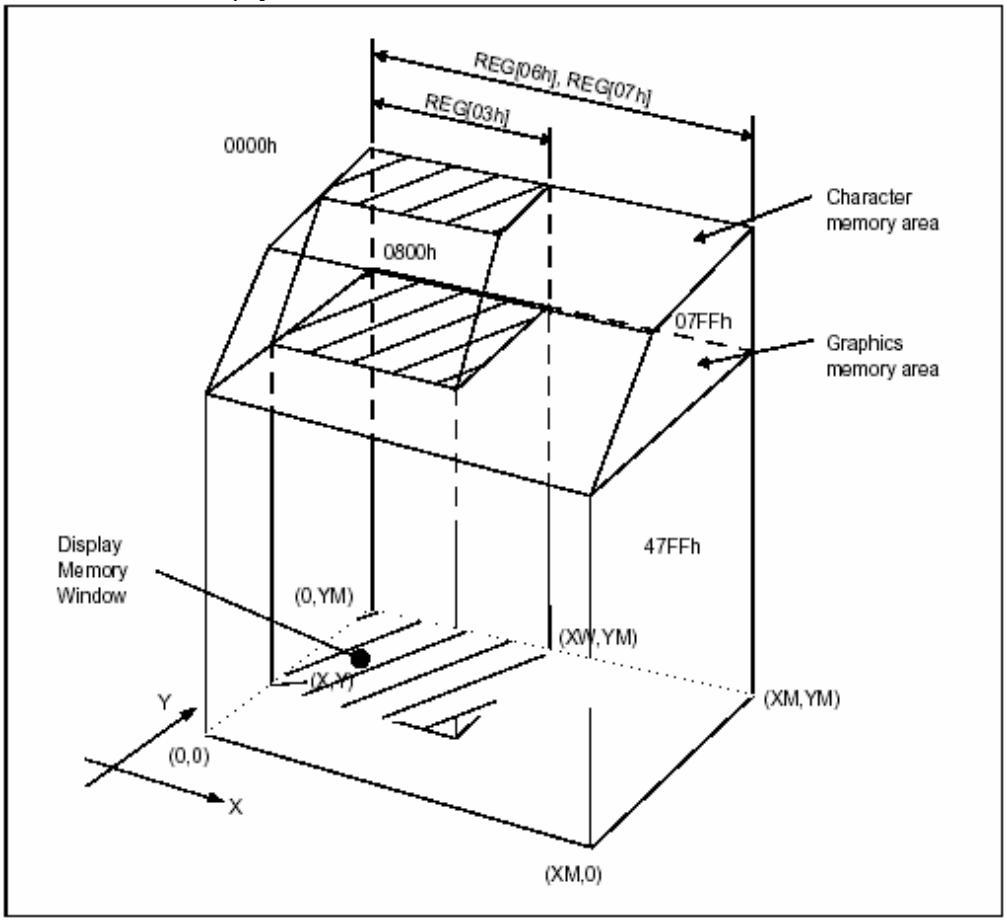


Figure 8-13 Virtual and Physical Screen Relationship

● **Display Address Scanning**

The S1D13700F01 scans the display memory in the same way as a raster scan CRT screen. Each row is scanned from left to right until the address range equals C/R, REG[03h] bits 7-0. rows are scanned from top to bottom. When in graphics mode, at the start of each line the address counter is set to the address at the start of the previous line plus the horizontal address range (or address pitch), REG[06h] – REG[07h].

In text mode, the address counter is set to the same start address, and the same character data is read, for each row in the character bitmap. However, a new row of the character generator output is used each time. Once all the rows in the character bitmap have been displayed, the address counter is set start address plus the horizontal address range (or address pitch) and the next line of text is displayed.

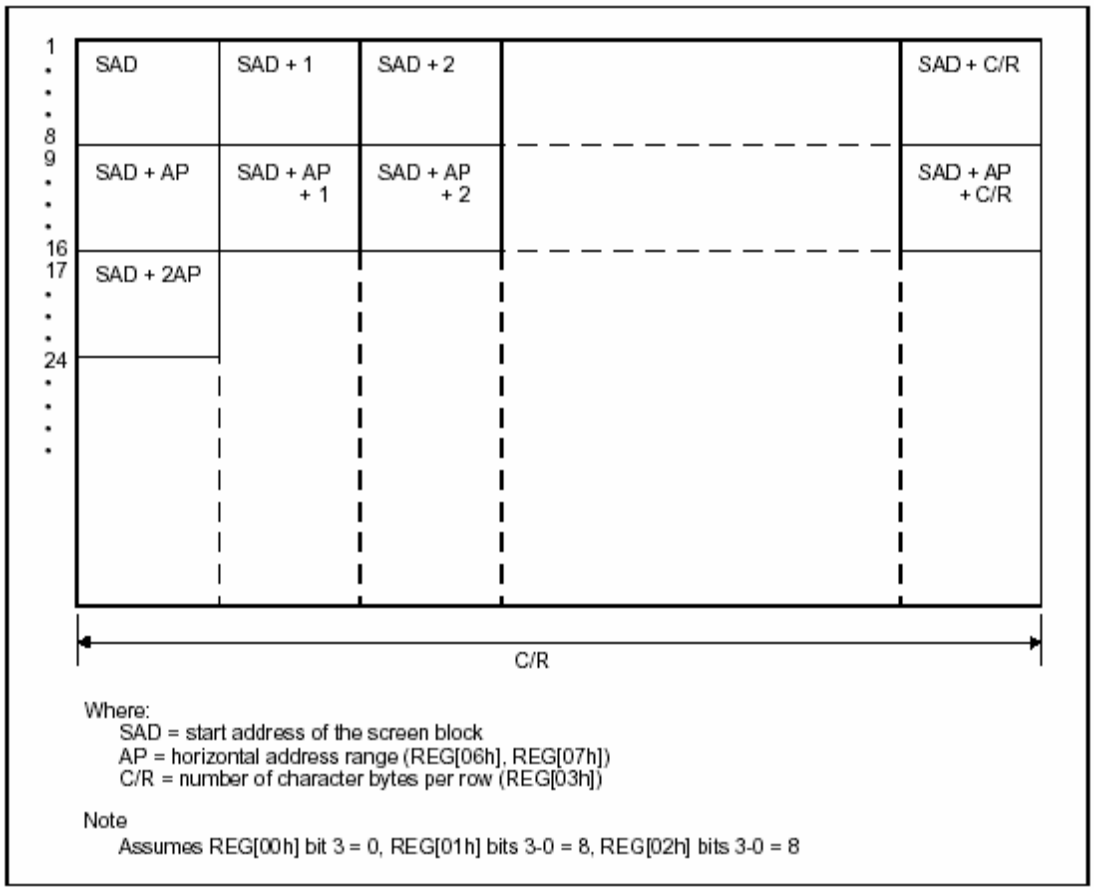


Figure 8-14 Display Address in Text Mode Example

Note:

One byte of display memory corresponds to one character

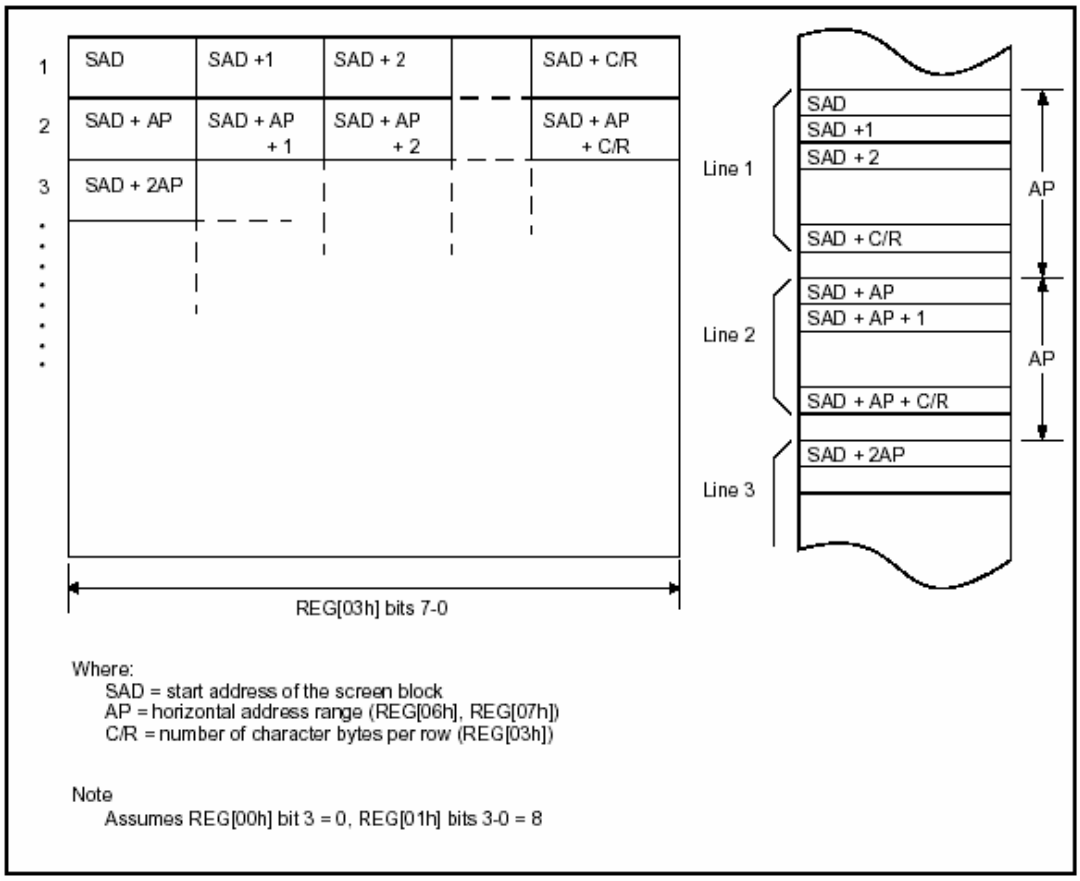


Figure 8-15 Display Address in Graphics Mode Example

Note:

In 1 bpp, one bit of display memory corresponds to one pixel, therefore, 1 byte of display memory corresponds to 8 pixels. In 2 bpp, 1 byte corresponds to 4 pixels. In 4 bpp, 1 byte corresponds to 2 pixels.

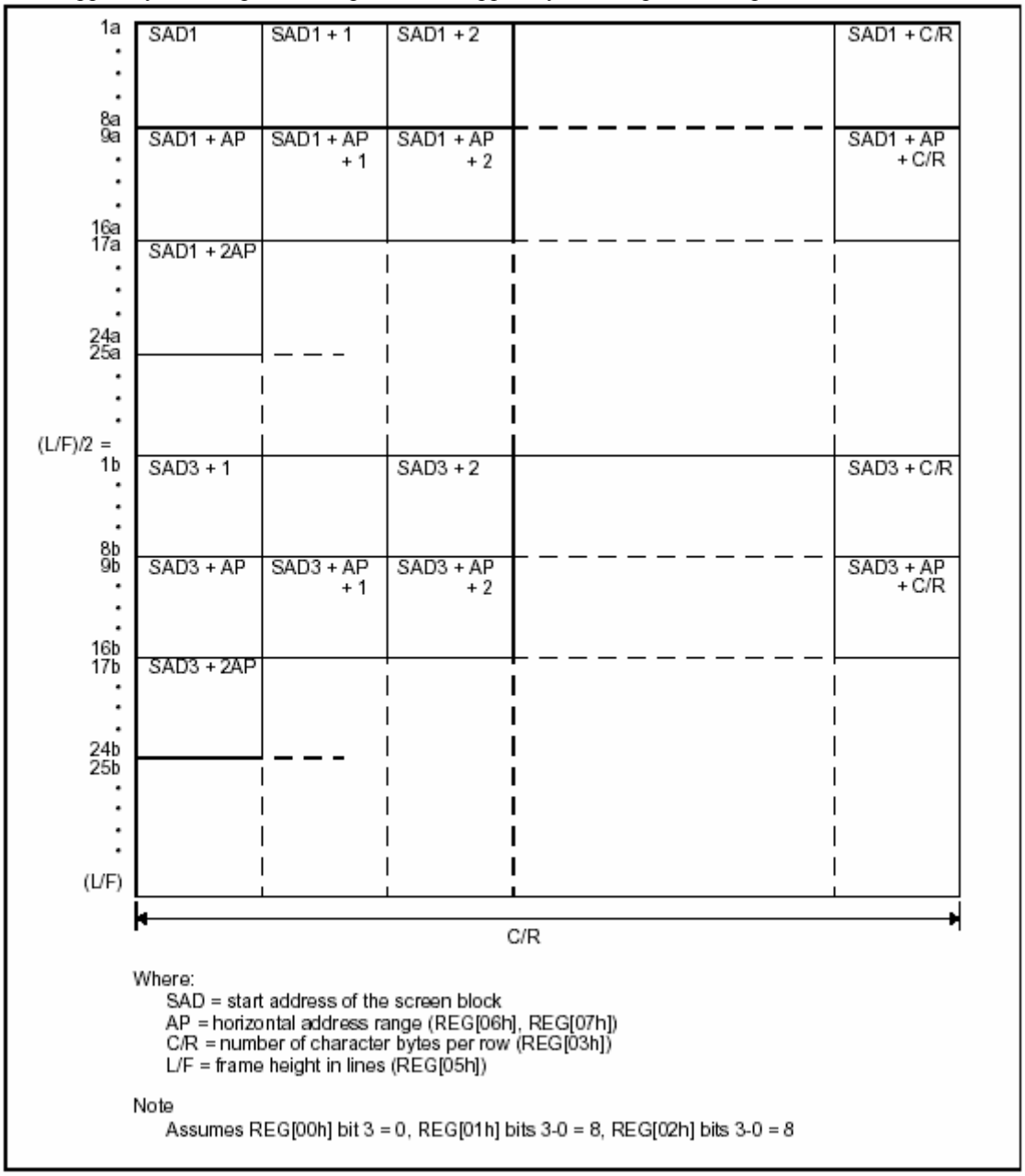


Figure 8-16 Dual Panel Display Address Indexing in Text Mode

Note:

In dual panel drive, the S1D13700F01 reads line 1a and line 1b as one cycle. The upper and lower panels are thus read alternately, one line at a time.

- **Display Scan Timing**

During display scanning, the S1D13700F01 pauses at the end of each line for TC/R – C/R ((REG[04h] bits 7-0 – (REG[03h] bits 7-0)) display memory read cycles, although the LCD drive signals are still generated. TC/R may be set to any value within the constraints imposed by C/R, input clock (CLK), f_{FR}, and the size of the LCD panel. This pause may be used to fine tune the frame frequency. Alternately, the microprocessor may use this pause to access the display memory data.

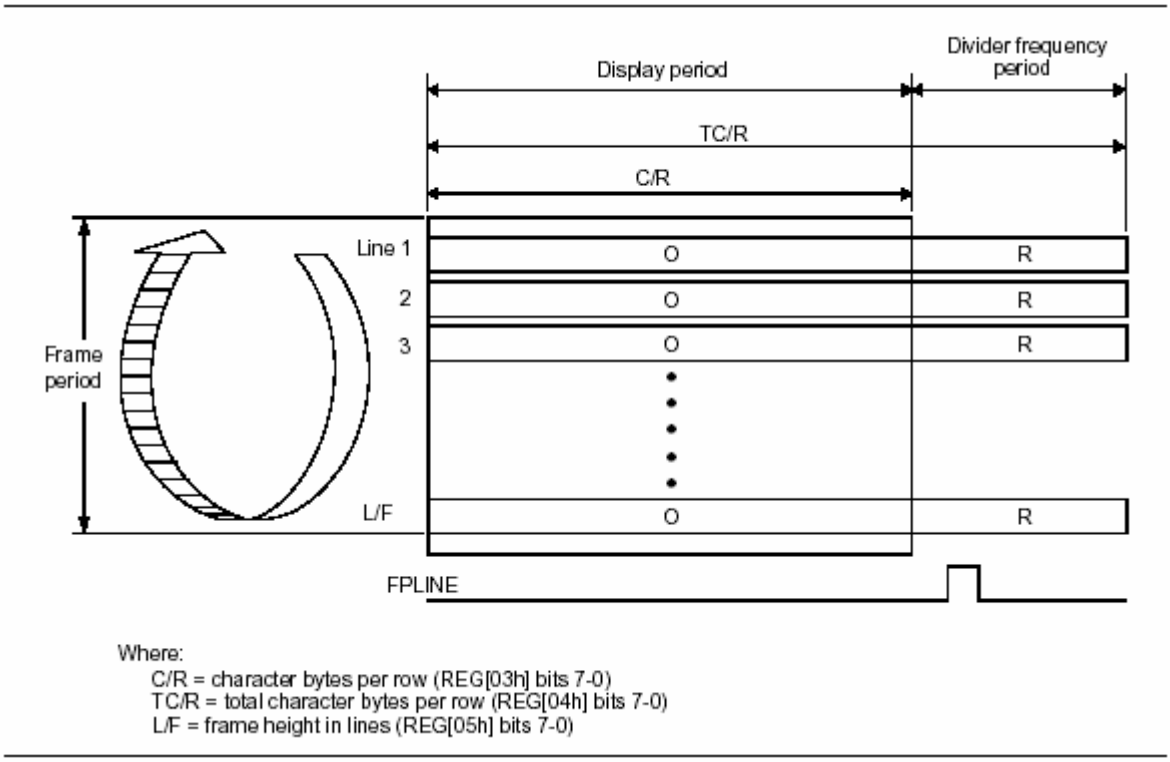


Figure 8-17 Relationship between Total character bytes per row and character bytes per row

Note

The divider adjustment interval (R) applies to both the upper and lower screens even if a dual panel drive is selected, REG[00h] bit 3 = 1. In this case, FPLINE is active only at the end of the lower screen's display interval.

8-7 Cursor Control

- **Cursor Write Register Function**

The cursor write register (REG[1Ch] – REG[1Dh]) functions as both the displayed cursor position address register and, in indirect addressing mode, the display memory access address register. When accessing display memory outside the actual visible screen memory, the cursor write register should be saved before accessing the memory and then restored after the memory access is complete. This is done to prevent the cursor from visibly disappearing outside the display area.

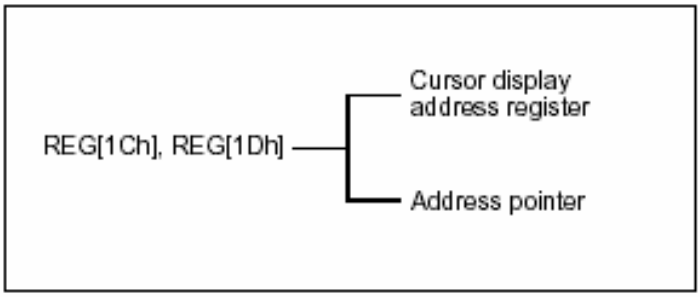


Figure 8-18 Cursor Address

The cursor may disappear from the display if the cursor address remains outside the displayed screen memory for more than a few hundred milliseconds.

- **Cursor Movement**

On each memory access, the cursor write register (REG[1Ch] – REG[1Dh]) is changed by the amount specified by the CSRDIR command (see REG[17h] bits 1-0) which automatically moves the cursor to the desired location.

- **Cursor Display Layers**

Although the S1D13700F01 can display up to three layers, the cursor is displayed in only one of these layers. For a two layer configuration (REG[18h] bit 4 = 0), the cursor is displayed in the first layer (L1). For a three layer configuration (REG[18h] bit 4 = 1), the cursor is displayed in the third layer (L3).

The cursor is not displayed if the address is moved outside of the memory for its layer. If it is necessary to display the cursor in a layer other than the present one, the layers may be swapped, or the cursor layer can be moved within the display memory.

Although the cursor is normally displayed for character data, the S1D13700F01 may also display a dummy cursor for graphical characters. This is only possible graphics screen is displayed, the text screen is turned off, and the microprocessor generates the cursor control address.

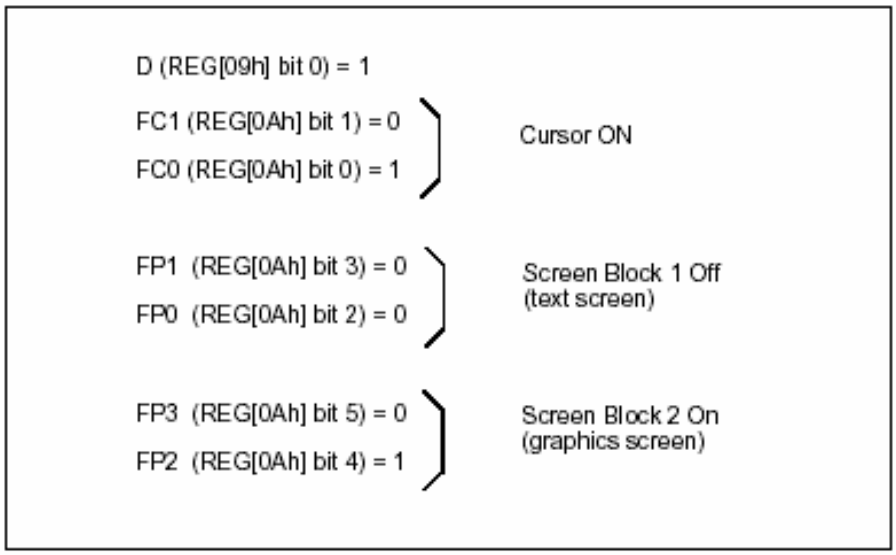


Figure 8-19 Cursor Display Layers

For example, if Chinese characters are displayed on a graphics screen, the cursor address is set to the second screen block in order to write the "graphics" display data. However, the cursor is not displayed. To display the cursor, the cursor address must be set to an address within the blank text screen block.

Since the automatic cursor increment is in address units, not character units, the controlling microprocessor must set the cursor write register (REG[1Ch] – REG[1Dh]) when moving the cursor over the graphical characters.

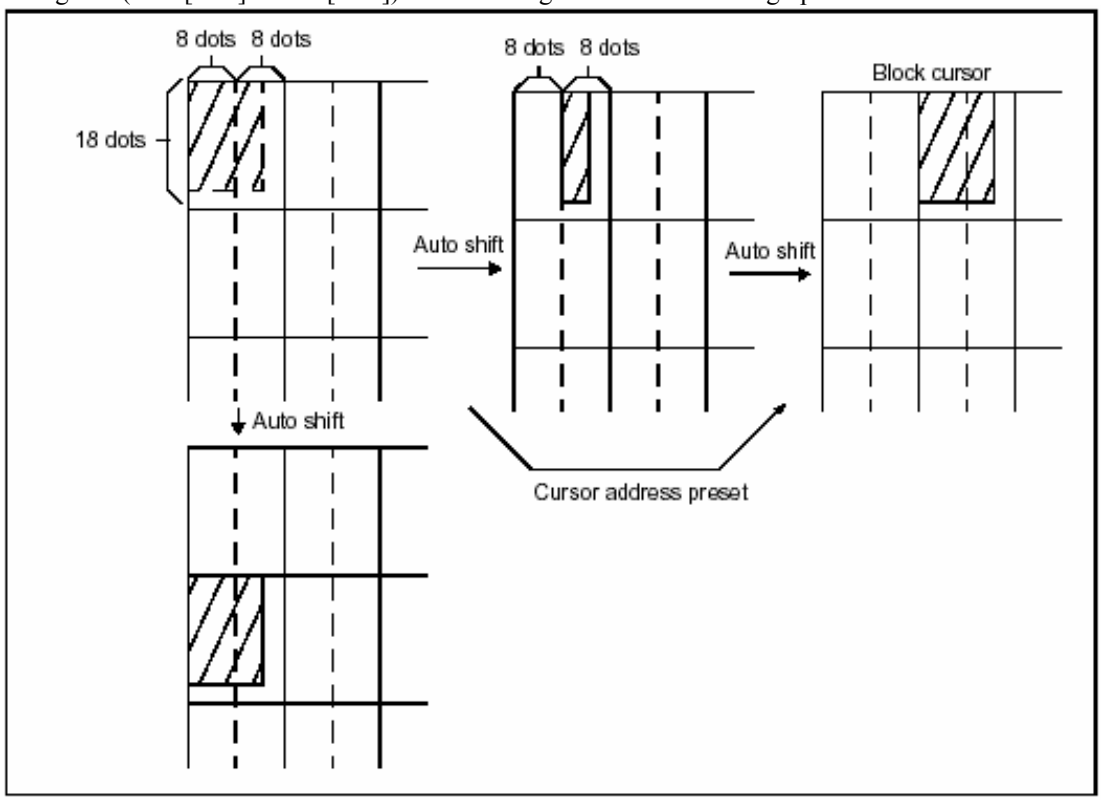


Figure 8-20 Cursor Movement

If no text screen is displayed, only a bar cursor can be displayed at the cursor address.

If the first layer is a mixed text and graphics screen and the cursor shape is set to a block cursor, the S1D13700F01 automatically decides which cursor shape to display. On the text screen it displays a block cursor, and on the graphic screen, a bar cursor.

- **Memory to Display Relationship**

The S1D13700F01 supports virtual screens that are larger than the physical size of the LCD panel address range (C/R), REG[03h] 7-0. a layer of the S1D13700F01 can be considered as a window into the larger virtual screen held in display memory. This window can be divided in to two blocks, with each block able to display a different portion of the virtual screen.

For example, this allows one block to dynamically scroll through a data area while the other block is used as a status message display area.

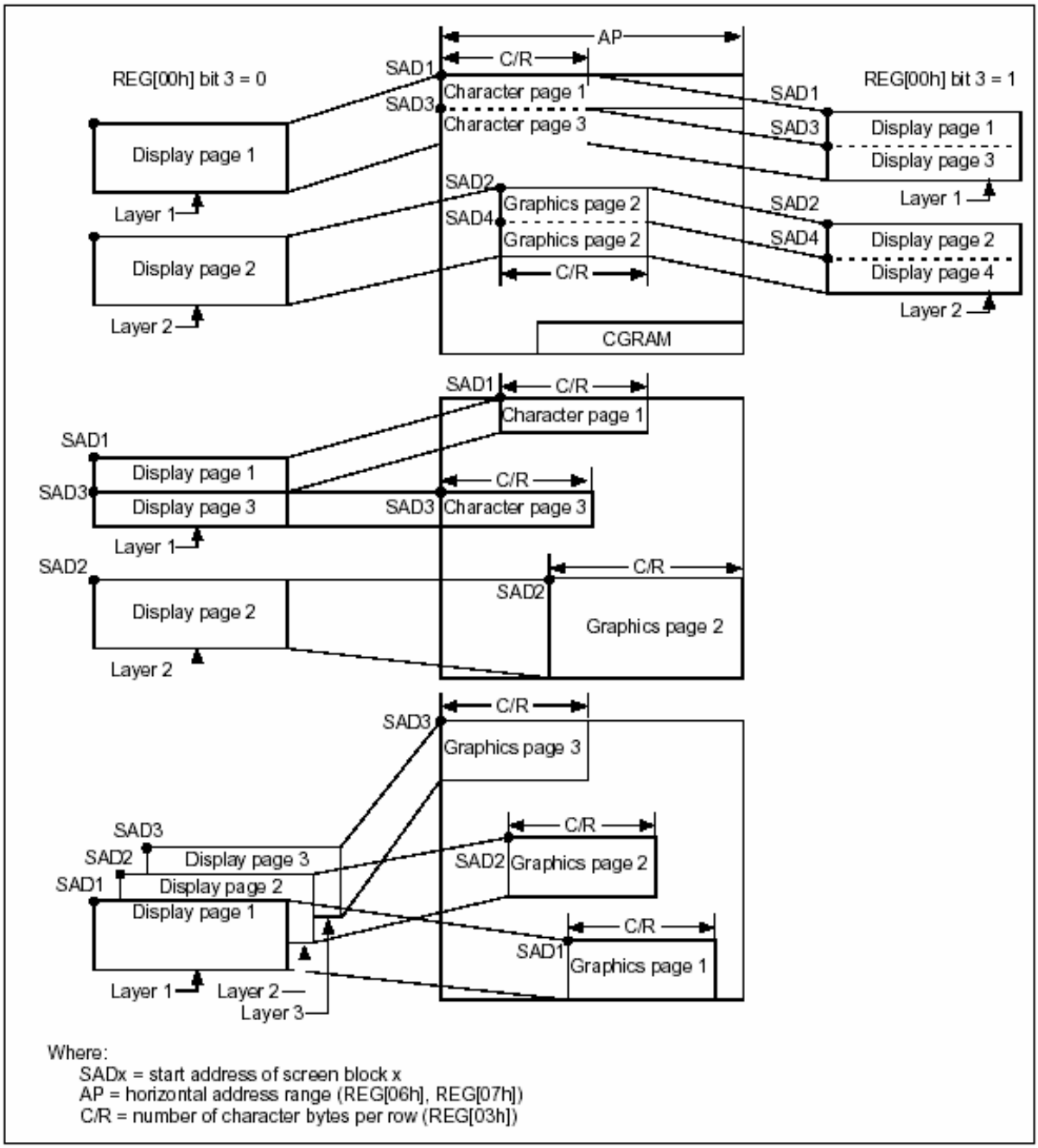


Figure 8-21 screen layers and memory relationship

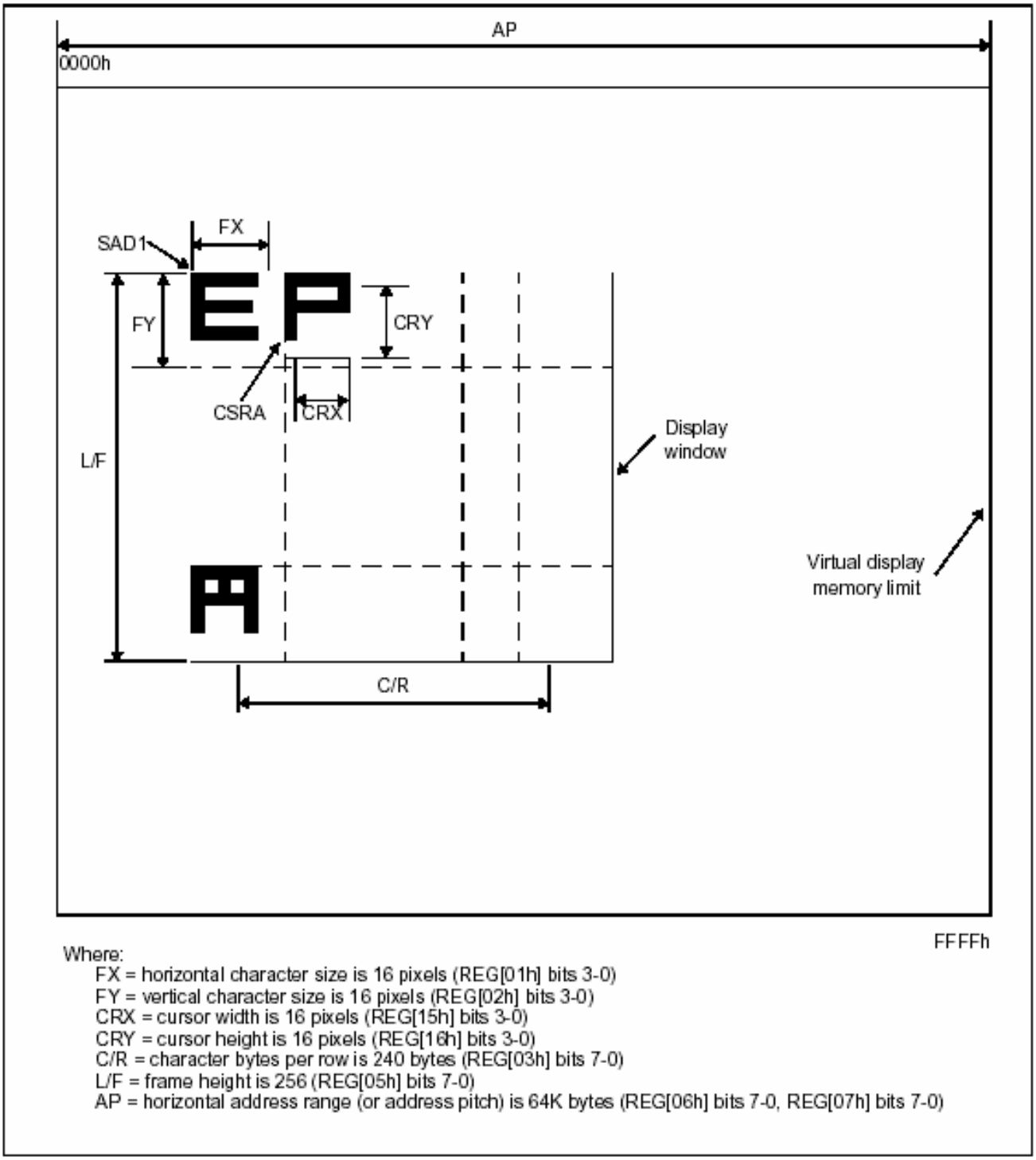


Figure 8-22 Virtual Display (Display Window to Memory Relationship)

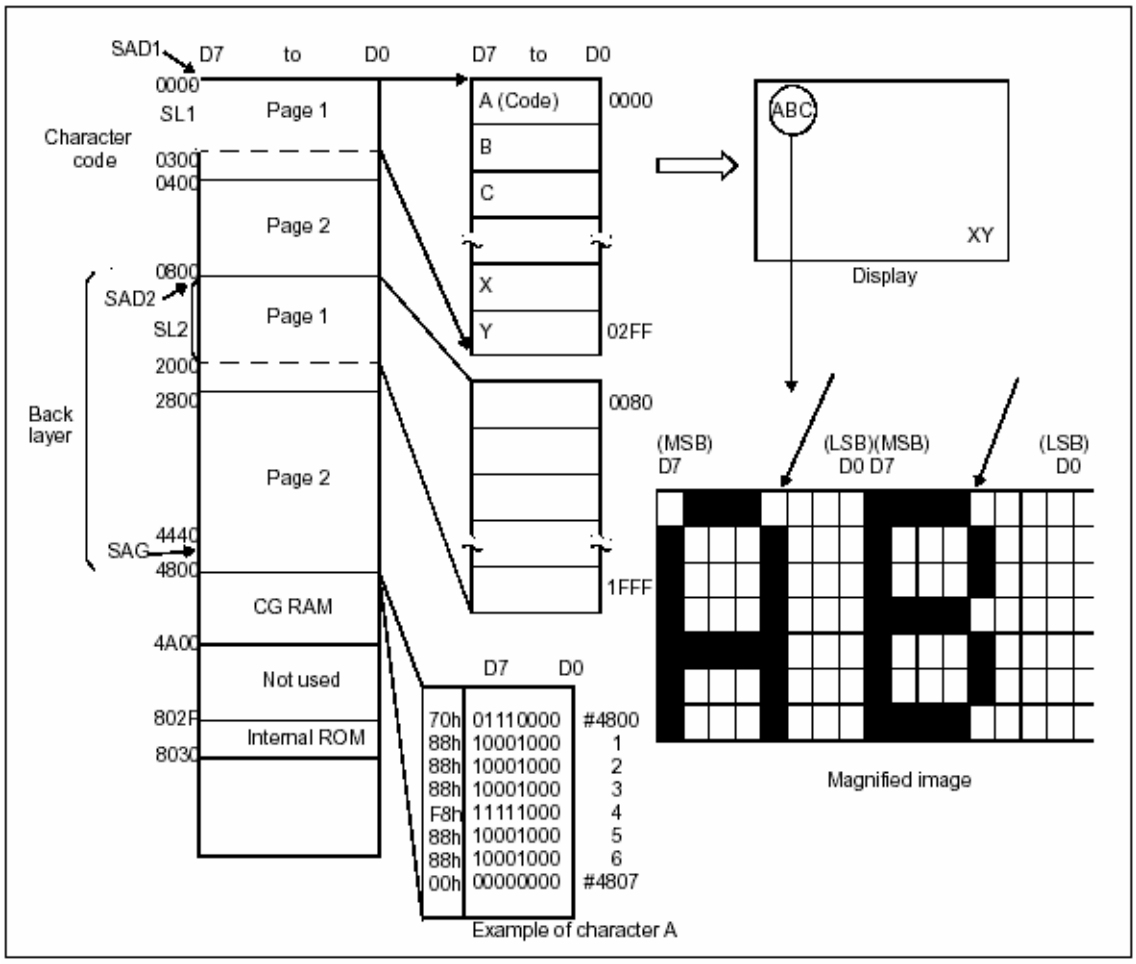


Figure 8-23 Memory Map and Magnified Characters.

8-8 Scrolling

The microprocessor can control A1D13700F01 scrolling modes by writing the scroll address registers for each screen block, REG[0Bh] – REG[14h]. This is referred to as address scrolling and can be used for both text and graphic screen blocks, if the display memory capacity is greater than one screen.

- **On-Page Scrolling**

The normal method of scrolling within a page is to move the whole display up one line and erase the bottom line. However, the S1D13700F01 does not automatically erase the bottom line, so it must be erased with blanking data when changing the scroll address register.

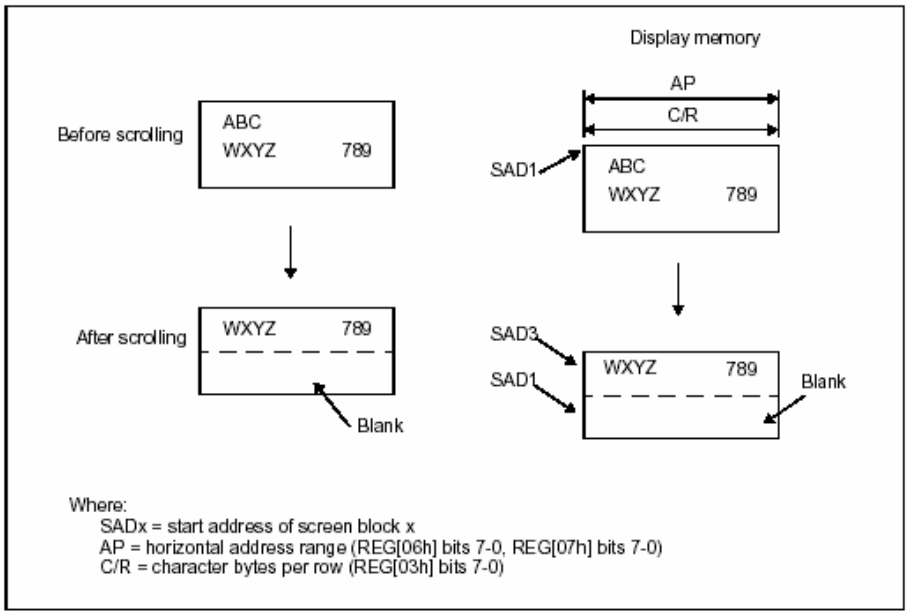


Figure 8-24 On-Page Scrolling

- **Inter-Page Scrolling**

Scrolling between pages and page switching can be performed only if the display memory capacity is greater than one screen. To scroll down one line / character, add the value of the horizontal address range (or address pitch), REG[06h] – REG[07h], to the current SADx. To scroll up, subtract the value of the horizontal address range form SADx.

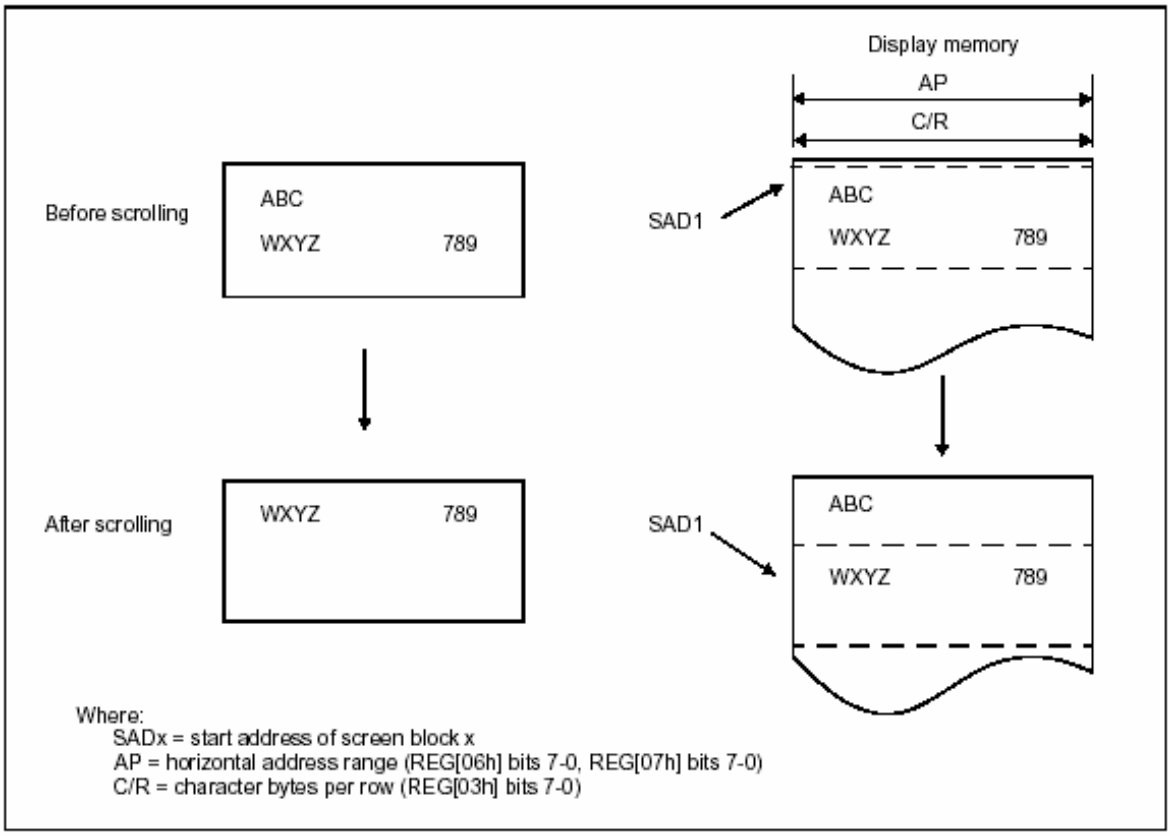


Figure 8-25 Inter-Page Scrolling

- **Horizontal Wraparound Scrolling**

For screen block in text mode, the display can be scrolled horizontally in one character units, regardless of the display memory capacity

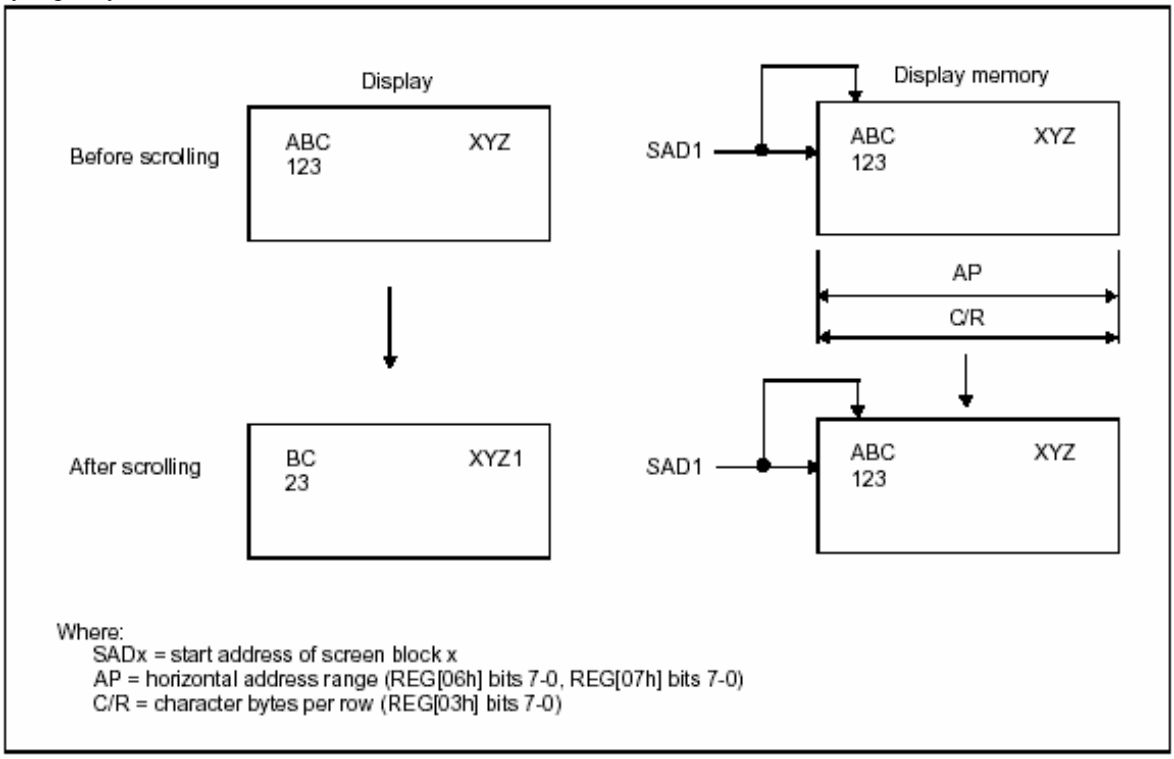


Figure 8-26 Horizontal Wraparound Scrolling

- **Bi-directional Scrolling**

Bi-directional scrolling can be performed only if the display memory is larger than the physical screen in both the horizontal (REG[06h], REG[07h] >REG[03h] and vertical directions. Scrolling is normally done in single-character units, however the HDOT SCR command (see REG[1Bh] bits 2-0) allows horizontal scrolling in pixel units (for text blocks only). Single pixel horizontal scrolling can be performed using both the SCROLL and HDOT SCR commands.

Note

In 2 bpp and 4 bpp grayscale mode REG[1Bh] bits 2-0 (HODT SCR) must be set to 0, so horizontal scrolling can only be done in single character units (not pixel units).

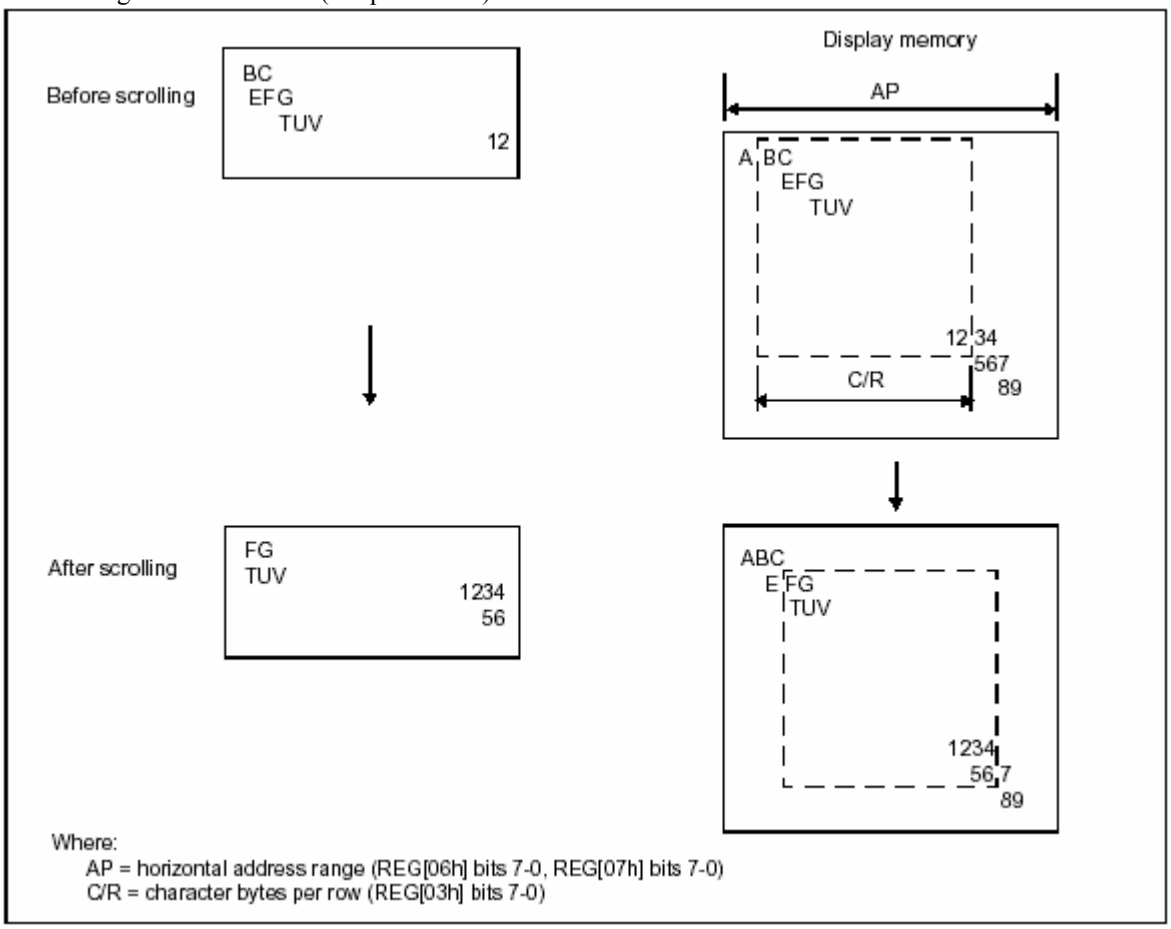


Figure 8-27 Bi-Directional Scrolling

- **Scroll Units**

The following table summarizes the units, or steps, that can be scrolled for each mode.

Table 8-27 Scrolling Unit Summary

mode	Vertical	Horizontal
Graphic	Pixels	Pixels

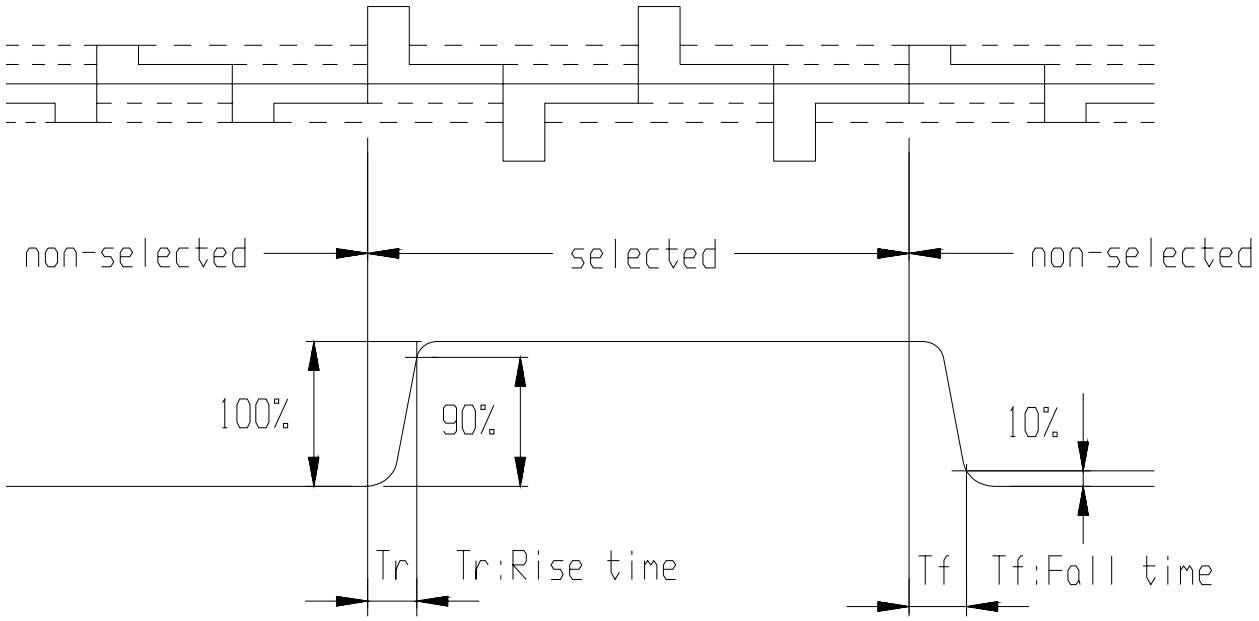
Note

In a divided screen, each block cannot be independently scrolled horizontally in pixel units.

9. ELECTRO-OPTICAL CHARACTERISTICS (V_{OP} = 23.0V, Ta = 25°C)

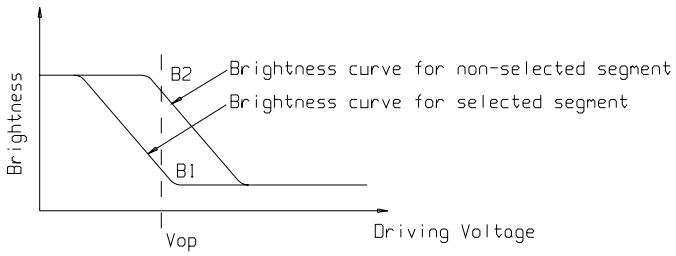
Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks	Note
Response time	Tr	---	---	318	---	ms	---	1
	Tf	---	---	99	---	ms	---	1
Contrast ratio	Cr	---	---	20.1	---	---	---	2
Viewing angle range	θ	Cr ≥ 2	35	---	---	deg	∅ = 90°	3
			32	---	---	deg	∅ = 270°	3
			38	---	---	deg	∅ = 0°	3
			60	---	---	deg	∅ = 180°	3

Note1: Definition of response time.

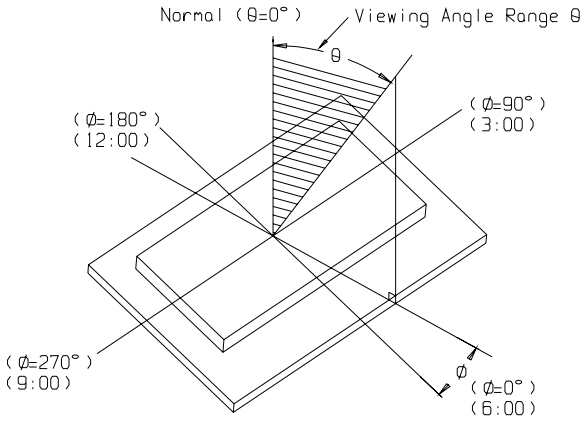


Note2: Definition of contrast ratio 'Cr' .

$$Cr = \frac{\text{Brightness of non-selected segment(B2)}}{\text{Brightness of selected segment(B1)}}$$



Note3: Definition of viewing angle range 'θ'.



10. INTERFACE PIN CONNECTIONS

Pin No.	Symbol	Level	Description
1	VSS	0V	Ground
2	VDD	5.0V	Supply voltage for logic
3	VEE	-20V	LCD supply voltage
4	VO	---	Contrast adjust
5	/WR	L	Write strobe for MPU interface
6	/RD	L	Read strobe for MPU interface
7	/CS	L	Chip select for MPU interface
8	/WAIT	---	Wait output for MPU interface
9	/RESET	L	Reset input
10	AB0	---	Command or Parameter
11	D0	H/L	Data bit 0
12	D1	H/L	Data bit 1
13	D2	H/L	Data bit 2
14	D3	H/L	Data bit 3
15	D4	H/L	Data bit 4
16	D5	H/L	Data bit 5
17	D6	H/L	Data bit 6
18	D7	H/L	Data bit 7
19	BLA	4.0V	Back light anode
20	BLK	0V	Back light cathode

The default setting of this module is 80 series, if change R23 to 10Kohm and let R24 open, this module will change to 68 series.

11. BACK LIGHT SPECIFICATION

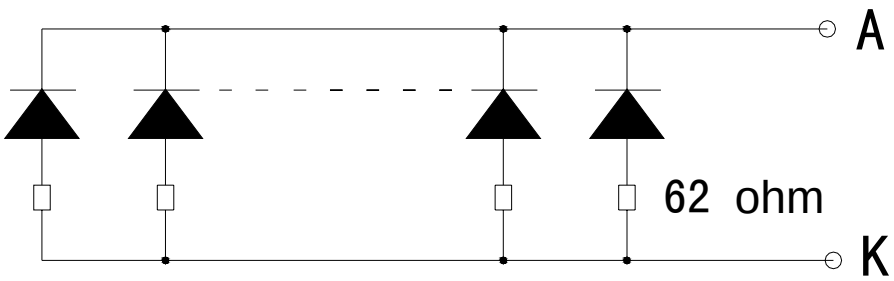
11-1. ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	Condition	Rating	Unit
Reverse Voltage	Vr		5	V
Reverse Current	Ir		600	μA
Absolute maximum forward current	Ifm		300	mA
Peak forward current	Ifp	Imsec plus 10% Duty cycle	900	mA
Power dissipation	Pd		1500	mW
Operating temperature range	Top		-20~+70	℃
Storing temperature	Tst		-30~+80	℃

11-2. ELECTRICAL/OPTLCAL CHARACTERISTICS (Ta=25℃,If=160MA)

Color	Peak wavelength λp(nm)	Spectral line half width Δλ (nm)	Operating voltage(V) (±0.25V)	Forward Current(mA)
White			4.0	160

11-3. BLOCK DIAGRAM (1X12=12dies LED)



12. RELIABILITY

12-1. Content of Reliability Test

Environmental Test				
No.	**Test Item**	**Content of Test**	**Test Condition**	**Applicable Standard**
1	High temperature storage	Endurance test applying the high storage temperature for a long time.	60 °C 96 hrs	------
2	Low temperature storage	Endurance test applying the low storage temperature for a long time.	-10 °C 96 hrs	------
3	High temperature operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	50 °C 96 hrs	------
4	Low temperature operation	Endurance test applying the electric stress under low temperature for a long time.	0 °C 96 hrs	------
5	High temperature / Humidity storage	Endurance test applying the high temperature and high humidity storage for a long time.	60 °C , 90 %RH 24 hrs	MIL-202E-103B JIS-C5023
6	High temperature / Humidity operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	50 °C , 90 %RH 24 hrs	MIL-202E-103B JIS-C5023
7	Temperature cycle	Endurance test applying the low and high temperature cycle. 0°C 30min ⇌ 25°C 5min. ⇌ 50°C 30min 1 cycle	0°C /50°C 10 cycles	------
Mechanical Test				
8	Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz → 1.5mmp-p 22~500Hz → 1.5G Total 0.5hrs	MIL-202E-201A JIS-C5025 JIS-C7022-A-10
9	Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G half sign wave 11 msedc 3 times of each direction	MIL-202E-213B
10	Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115 mbar 40 hrs	MIL-202E-105C
Others				
11	Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V , RS=1.5 kΩ CS=100 pF 1 time	MIL-883B-3015.1

*** Supply voltage for logic system = 5.0V. Supply voltage for LCD system = Operating voltage at 25°C.

12-2. Failure Judgment Criterion

Criterion Item	**Test Item No.**											**Failure Judgment Criterion**
	1	2	3	4	5	6	7	8	9	10	11	
Basic specification												Out of the Basic Specification
Electrical characteristic												Out of the DC and AC Characteristic
Mechanical characteristic												Out of the Mechanical Specification Color change : Out of Limit Appearance Specification
Optical characteristic												Out of the Appearance Standard

13. QUALITY GUARANTEE

13-1. Acceptable Quality Level

Each lot should satisfy the quality level defined as follows.

- Inspection method: MIL-STD-105E LEVEL II Normal one time sampling
- AQL

Partition	AQL	Definition
A: Major	0.4%	Functional defective as product
B: Minor	1.5%	Satisfy all functions as product but not satisfy cosmetic standard

13-2. Definition of 'LOT'

One lot means the delivery quantity to customer at one time.

13-3. Conditions of Cosmetic Inspection

- Environmental condition

The inspection should be performed at the 1m of height from the LCD module under 2 pieces of 40W white fluorescent lamps (Normal temperature 20~25°C and normal humidity 60±15%RH).

- Inspection method

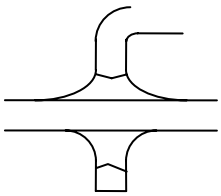
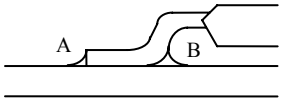
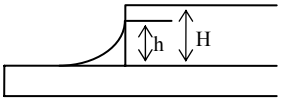
The visual check should be performed vertically at more than 30cm distance from the LCD panel.

- Driving voltage

The Vo value which the most optimal contrast can be obtained near the specified Vo in the specification. (Within ±0.5Vof the typical value at 25°C.).

14. INSPECTION CRITERIA

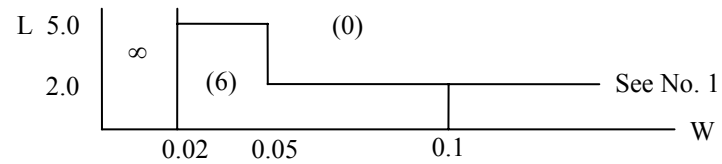
14-1. Module Cosmetic Criteria

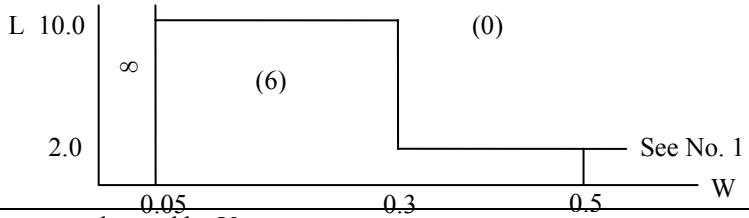
No.	Item	Judgment Criterion	Partition
1	Difference in Spec.	None allowed	Major
2	Pattern peeling	No substrate pattern peeling and floating	Major
3	Soldering defects	No soldering missing No soldering bridge No cold soldering	Major Major Minor
4	Resist flaw on substrate	Invisible copper foil (∅0.5mm or more) on substrate pattern	Minor
5	Accretion of metallic Foreign matter	No soldering dust No accretion of metallic foreign matters (Not exceed ∅0.2mm)	Minor Minor
6	Stain	No stain to spoil cosmetic badly	Minor
7	Plate discoloring	No plate fading, rusting and discoloring	Minor
8	Solder amount 1. Lead parts	a. Soldering side of PCB Solder to form a 'Filet' all around the lead. Solder should not hide the lead form perfectly. (too much) b. Components side (In case of 'Through Hole PCB') Solder to reach the Components side of PCB. 	Minor
	2. Flat packages	Either 'toe' (A) or 'heal' (B) of the lead to be covered by 'Filet'. Lead form to be assume over solder. 	Minor
	3. Chips	(3/2) H ≥ h ≥ (1/2) H 	Minor

14-2. Screen Cosmetic Criteria (Non-Operating)

<table>
<tr><th>No.</th><th>Defect</th><th>Judgment Criterion</th><th>Partition</th></tr>
<tr><td>1</td><td>Spots</td><td>In accordance with Screen Cosmetic Criteria (Operating) No.1.</td><td>Minor</td></tr>
<tr><td>2</td><td>Lines</td><td>In accordance with Screen Cosmetic Criteria (Operating) No.2.</td><td>Minor</td></tr>
<tr><td>3</td><td>Bubbles in polarizer</td><td><table><tr><th>Size : d mm</th><th>Acceptable Qty in active area</th></tr><tr><td>d ≤ 0.3</td><td>Disregard</td></tr><tr><td>0.3 < d ≤ 1.0</td><td>3</td></tr><tr><td>1.0 < d ≤ 1.5</td><td>1</td></tr><tr><td>1.5 < d</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>4</td><td>Scratch</td><td>In accordance with spots and lines operating cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.</td><td>Minor</td></tr>
<tr><td>5</td><td>Allowable density</td><td>Above defects should be separated more than 30mm each other.</td><td>Minor</td></tr>
<tr><td>6</td><td>Coloration</td><td>Not to be noticeable coloration in the viewing area of the LCD panels.
Back-lit type should be judged with back-lit on state only.</td><td>Minor</td></tr>
<tr><td>7</td><td>Contamination</td><td>Not to be noticeable.</td><td>Minor</td></tr>
</table>

14-3. Screen Cosmetic Criteria (Operating)

<table>
<tr><th>No.</th><th>Defect</th><th>Judgment Criterion</th><th>Partition</th></tr>
<tr><td>1</td><td>Spots</td><td>A) Clear<table><tr><th>Size : d mm</th><th>Acceptable Qty in active area</th></tr><tr><td>d ≤ 0.1</td><td>Disregard</td></tr><tr><td>0.1 < d ≤ 0.2</td><td>6</td></tr><tr><td>0.2 < d ≤ 0.3</td><td>2</td></tr><tr><td>0.3 < d</td><td>0</td></tr></table>Note: Including pin holes and defective dots which must be within one pixel size.
B) Unclear<table><tr><th>Size : d mm</th><th>Acceptable Qty in active area</th></tr><tr><td>d ≤ 0.2</td><td>Disregard</td></tr><tr><td>0.2 < d ≤ 0.5</td><td>6</td></tr><tr><td>0.5 < d ≤ 0.7</td><td>2</td></tr><tr><td>0.7 < d</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>2</td><td>Lines</td><td>A) Clear
 

Note : ( ) - Acceptable Qty in active area
L - Length (mm)
W - Width (mm)
∞ - Disregard
B) Unclear
 
</td><td>Minor</td></tr>
</table>

'Clear' = the shade and size are not changed by Vo.
'Unclear' = the shade and size are changed by Vo.

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Hong Kong Science Park, Pak Shek Kok, Tai Po, Hong Kong
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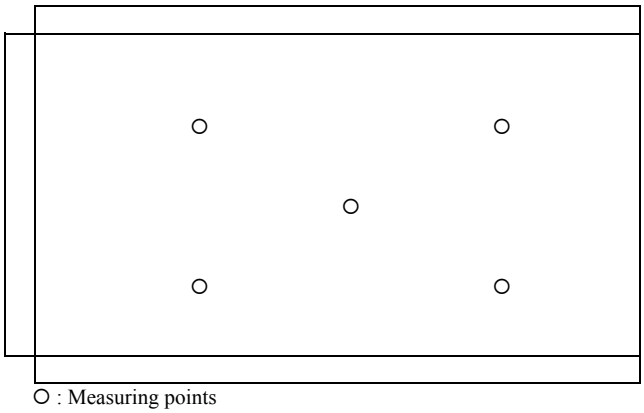
E-mail : sales@bonafide.com.hk Homepage : http://www.bonafide.com.hk

14-4. Screen Cosmetic Criteria (Operating) (Continued)

No.	Defect	Judgment Criterion	Partition
3	Rubbing line	Not to be noticeable.	
4	Allowable density	Above defects should be separated more than 10mm each other.	Minor
5	Rainbow	Not to be noticeable.	Minor
6	Dot size	To be 95% ~ 105% of the dot size (Typ.) in drawing. Partial defects of each dot (ex. pin-hole) should be treated as 'spot'. (see *Screen Cosmetic Criteria (Operating) No.1*)	Minor
7	Uneven brightness (only back-lit type module)	Uneven brightness must be BMAX / BMIN ≤ 2 - BMAX : Max. value by measure in 5 points - BMIN : Min. value by measure in 5 points Divide active area into 4 vertically and horizontally. Measure 5 points shown in the following figure.  ○ : Measuring points	Minor

Note:

(1) Size: d = (long length + short length) / 2

(2) The limit samples for each item have priority.

(3) Complexes defects are defined item by item, but if the numbers of defects are defined in above table, the total number should not exceed 10.

(4) In case of 'concentration', even the spots or the lines of 'disregarded' size should not allow. Following three situations should be treated as 'concentration'.

- 7 or over defects in circle of ∅5mm.
- 10 or over defects in circle of ∅10mm.
- 20 or over defects in circle of ∅20mm.

15. PRECAUTIONS FOR USING LCD MODULES

15-1. Handing Precautions

(1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it or impact.

(2) If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.

(3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

(4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

(5) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

(6) Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.

- Water
- Ketene
- Aromatic solvents

(7) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.

(8) Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the I/O cable or the backlight cable.

(9) Do not attempt to disassemble or process the LCD module.

(10) NC terminal should be open. Do not connect anything.

(11) If the logic circuit power is off, do not apply the input signals.

(12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

- Be sure to ground the body when handling the LCD modules.
- Tools required for assembling, such as soldering irons, must be properly grounded.
- To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions.
- The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

15-2. Storage Precautions

When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags (avoid high temperature / high humidity and low temperatures below 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

15-3. Others

Liquid crystals solidify under low temperature (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subject to a low temperature.

If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.

To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity etc., exercise care to avoid holding the following sections when handling the modules.

- Exposed area of the printed circuit board.
- Terminal electrode sections.

16. USING LCD MODULES

16-1. Liquid Crystal Display Modules

LCD is composed of glass and polarizer. Pay attention to the following items when handling.

(1) Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.

(2) Do not touch, push or rub the exposed polarizer with anything harder than an HB pencil lead (glass, tweezers, etc.).

(3) N-hexane is recommended for cleaning the adhesives used to attach front/rear polarizer and reflectors made of organic substances which will be damaged by chemicals such as acetone, toluene, ethanol and isopropyl alcohol.

(4) When the display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum benign. Do not scrub hard to avoid damaging the display surface.

(5) Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.

(6) Avoid contacting oil and fats.

(7) Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizer. After products are tested at low temperature they must be warmed up in a container before coming is contacting with room temperature air.

(8) Do not put or attach anything on the display area to avoid leaving marks on.

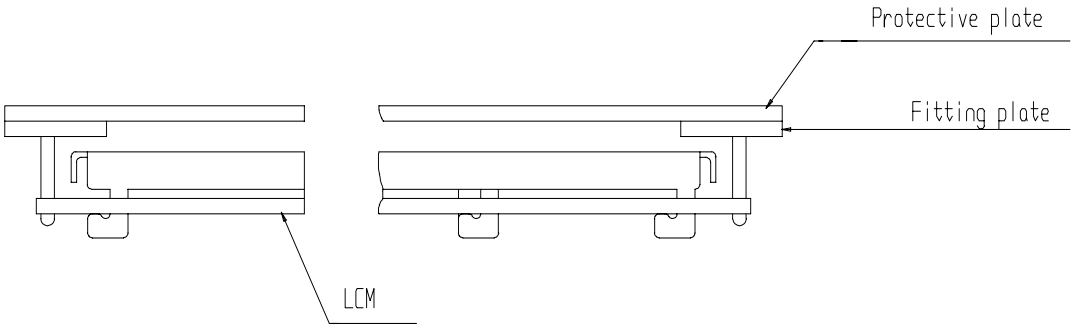
(9) Do not touch the display with bare hands. This will stain the display area and depredate insulation between terminals (some cosmetics are determinate to the polarizer).

(10) As glass is fragile. It tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring.

16-2. Installing LCD Modules

The hole in the printed circuit board is used to fix LCM as shown in the picture below. Attend to the following items when installing the LCM.

(1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be ±0.1mm.

16-3. Precaution for Handing LCD Modules

Since LCM has been assembled and adjusted with a high degree of precision, avoid applying excessive shocks to the module or making any alterations or modifications to it.

(1) Do not alter, modify or change the shape of the tab on the metal frame.

(2) Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.

(3) Do not damage or modify the pattern writing on the printed circuit board.

(4) Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector.

(5) Except for soldering the interface, do not make any alterations or modifications with a soldering iron.

(6) Do not drop, bend or twist LCM.

16-4. Electro-Static Discharge Control

Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

(1) Make certain that you are grounded when handing LCM.

(2) Before remove LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential.

(3) When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.

(4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced sparks coming from the commentator of the motor.

(5) As far as possible make the electric potential of your work clothes and that of the work bench the ground potential.

(6) To reduce the generation of static electricity is careful that the air in the work is not too dried. A relative humidity of 50%-60% is recommended.

16-5. Precaution for soldering to the LCM

(1) Observe the following when soldering lead wire, connector cable and etc. to the LCM.

- Soldering iron temperature: 280°C ± 10°C.
- Soldering time: 3-4 sec.
- Solder: eutectic solder.

If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage due to flux spatters.

(2) When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.

(3) When remove the electroluminescent panel from the PC board, be sure the solder has completely melted, the soldered pad on the PC board could be damaged.

16-6. Precautions for Operation

(1) Viewing angle varies with the change of liquid crystal driving voltage (V_O). Adjust V_O to show the best contrast.

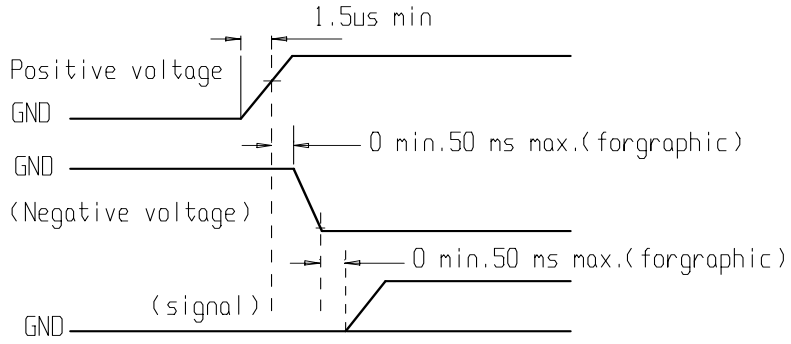
(2) Driving the LCD in the voltage above the limit shortens its life.

(3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.

(4) If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then back on.

(5) Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit. Therefore, it must be used under the relative condition of 40°C, 50% RH.

(6) When turning the power on, input each signal after the positive/negative voltage becomes stable.



16-7. Storage

When storing LCD as spares for some years, the following precaution are necessary.

(1) Store them in a sealed polyethylene bag. If properly sealed, there is no need for desiccant.

(2) Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0°C and 35°C.

(3) The polarizer surface should not come in contact with any other objects. (We advise you to store them in the container in which they were shipped.)

(4) Environmental conditions:

- Do not leave them for more than 168hrs. At 60°C.
- Should not be left for more than 48hrs. At -20°C.

16-8. Safety

(1) It is recommended to crush damaged or unnecessary LCD into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.

(2) If any liquid leaks out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

16-9. Limited Warranty

Unless agreed between BONA and customer, BONA will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with BONA LCD acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects must be returned to BONA within 90 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of BONA limited to repair and/or replacement on the terms set forth above. BONA will not be responsible for any subsequent or consequential events.

16-10. Return LCM under warranty

No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are:

- Broken LCD glass.
- PCB eyelet's damaged or modified.
- PCB conductors damaged.
- Circuit modified in any way, including addition of components.
- PCB tampered with by grinding, engraving or painting varnish.
- Soldering to or modifying the bezel in any manner.

Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB eyelet's, conductors and terminals.